Two Stage Operational Amplifier

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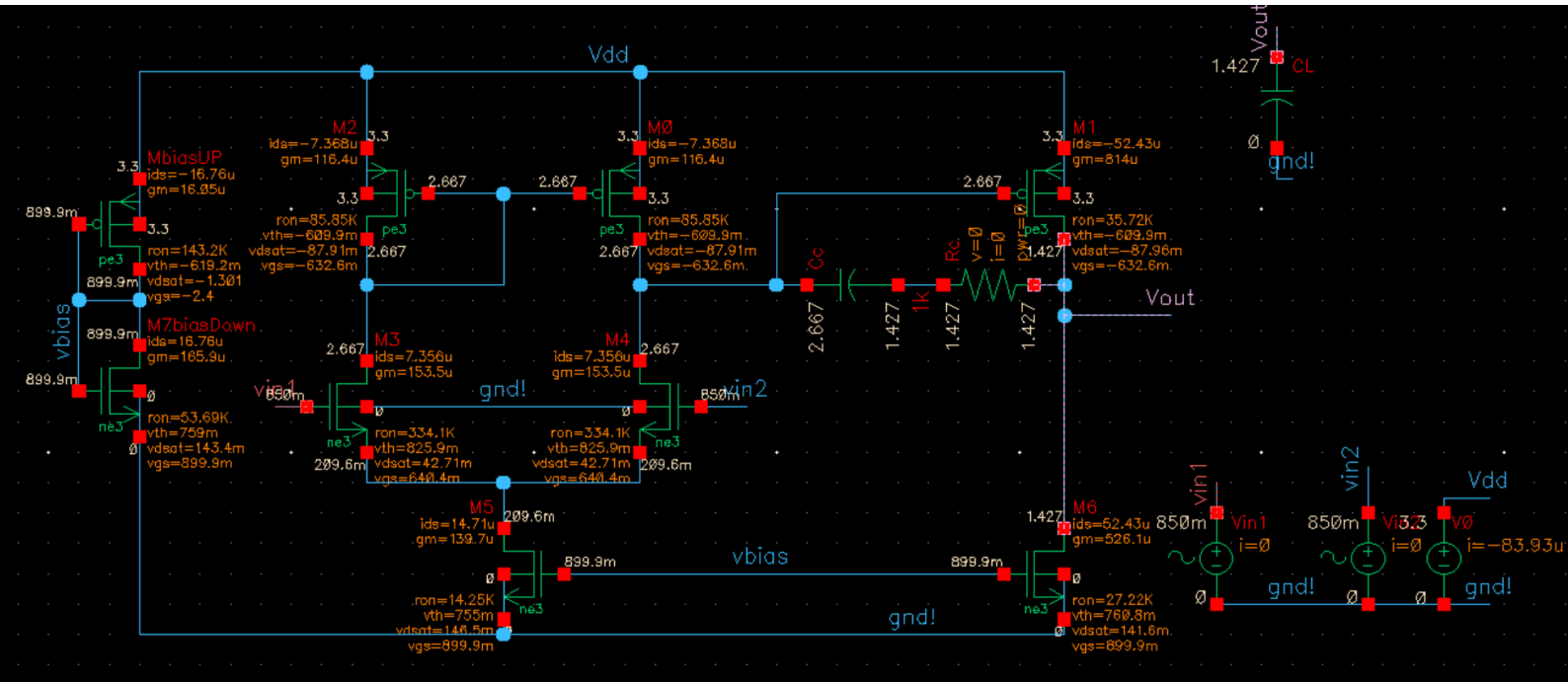
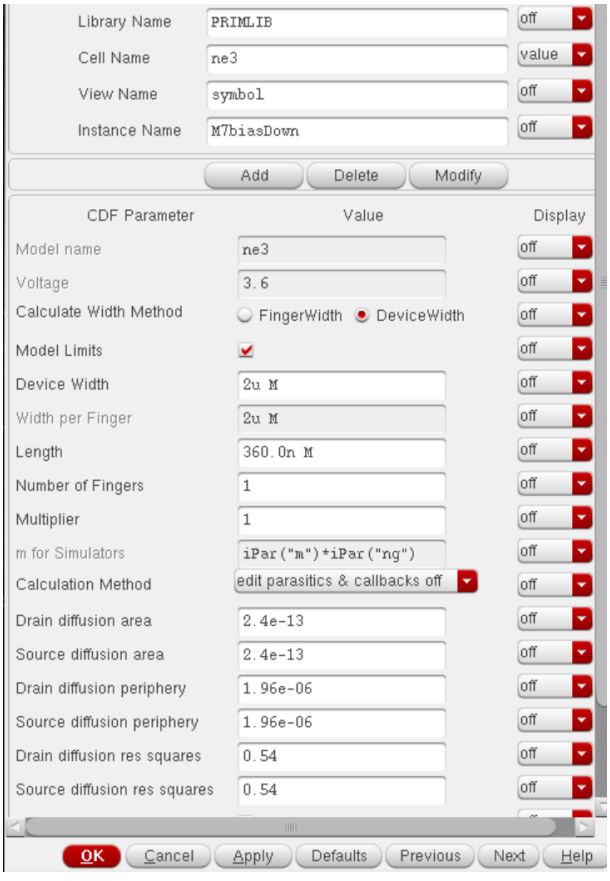
Schematic (Before Layout)

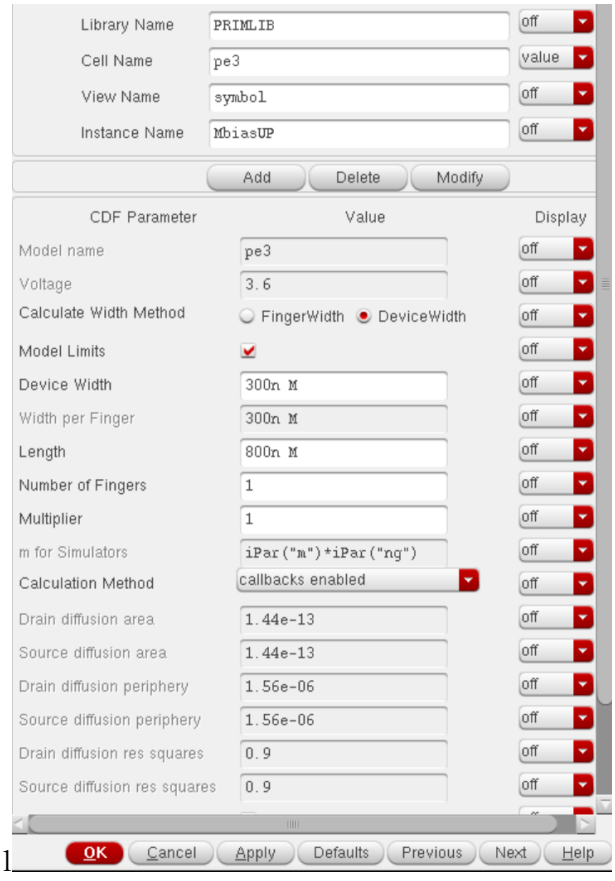


3.3 x 89.93µ = 296.769 µW ≈ 297 µW much less than 500 µW as required.
Cc = 2.5 pF > 2.2 pF = 0.22 x C_L thus PM > 60°
Also V_{bias} = 899.9 mV ≈ 0.9 V

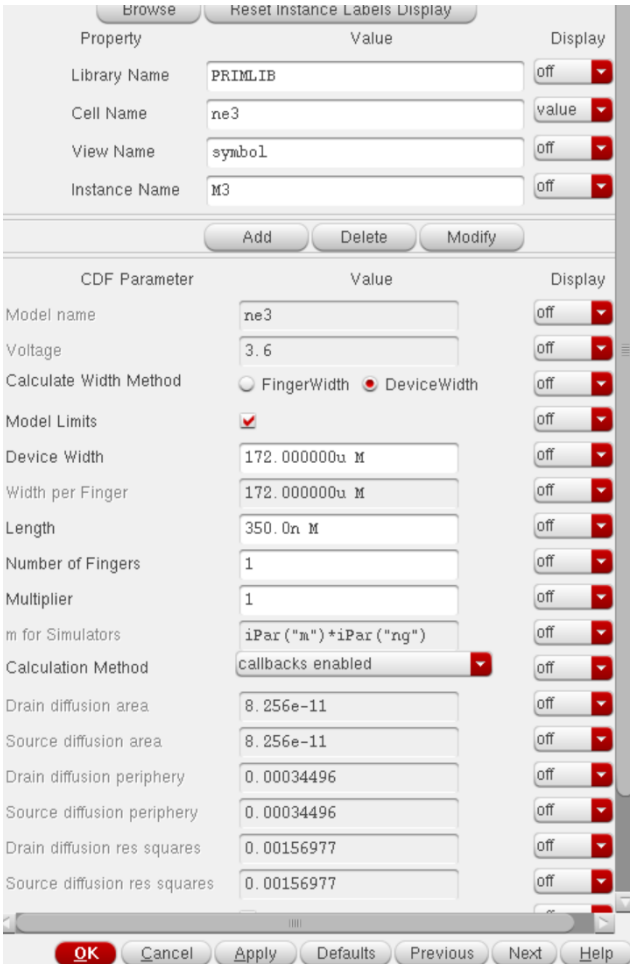
Transistor Properties



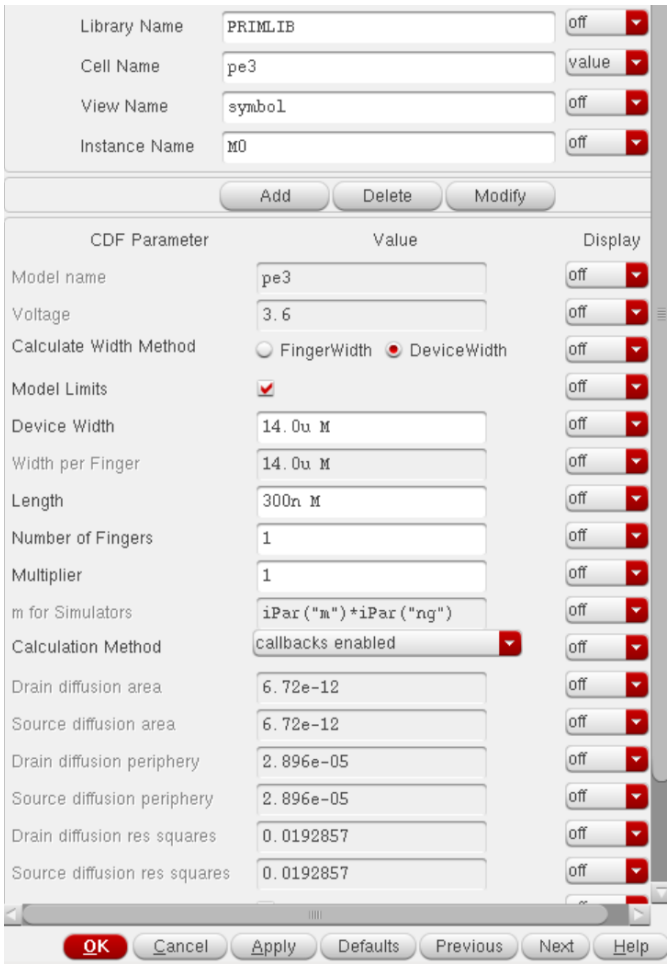
NMOS of bias circuit



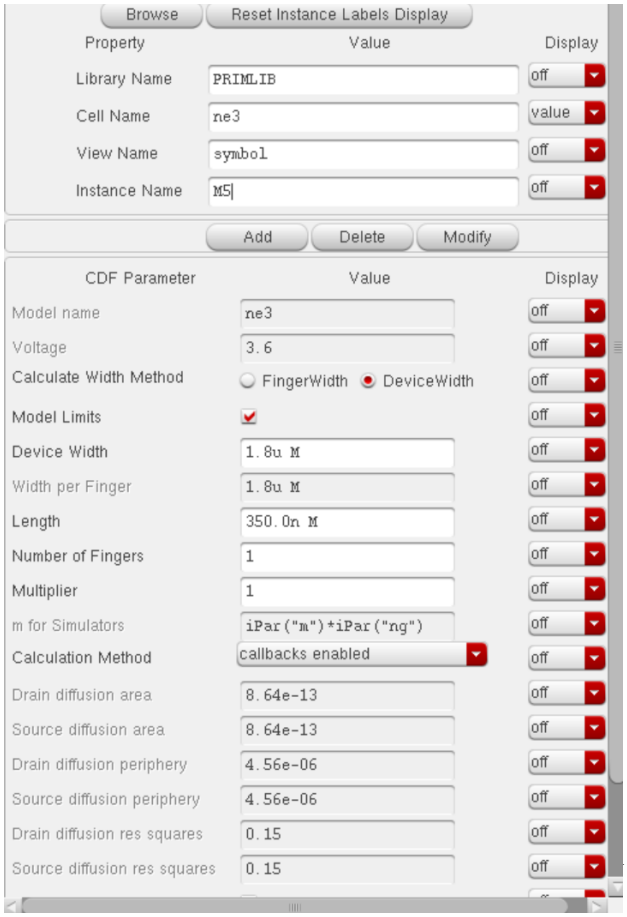
PMOS of bias circuit



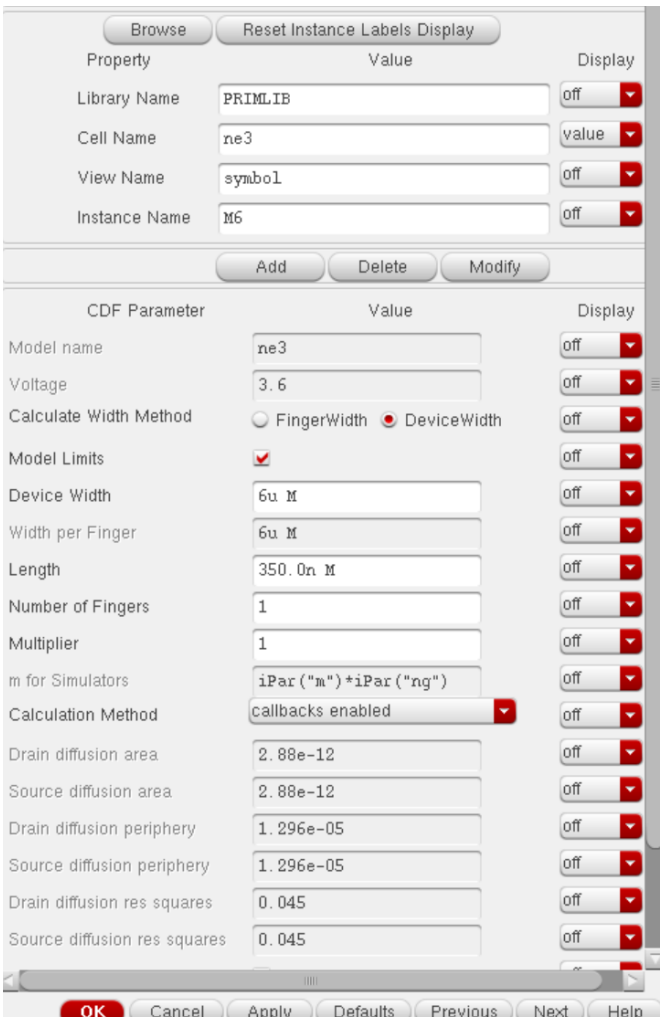
NMOS of first stage



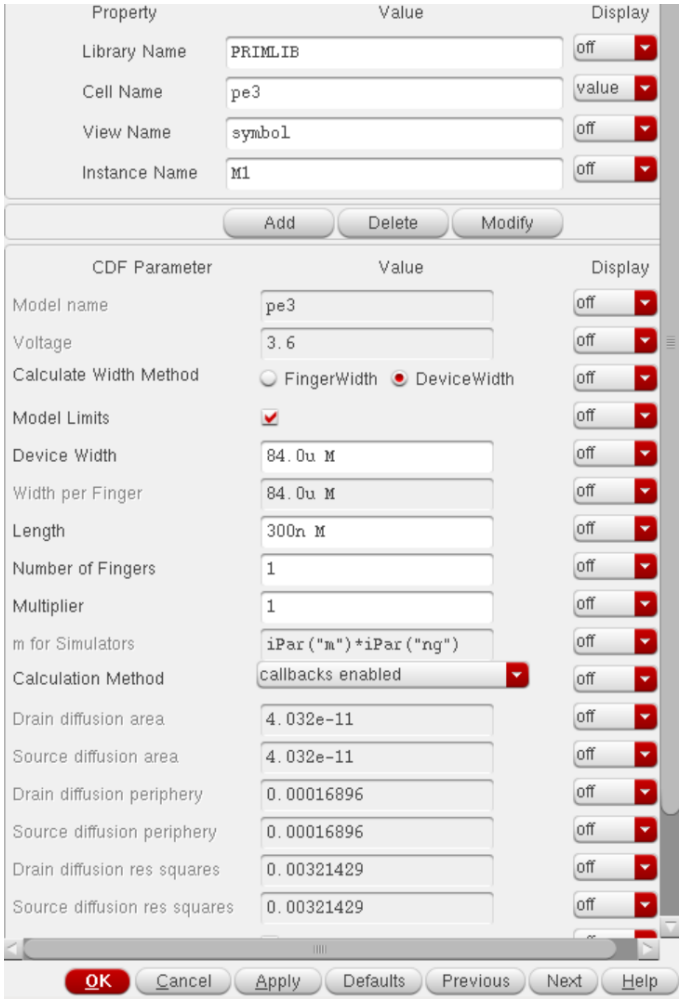
PMOS of first stage



Current Source of first stage



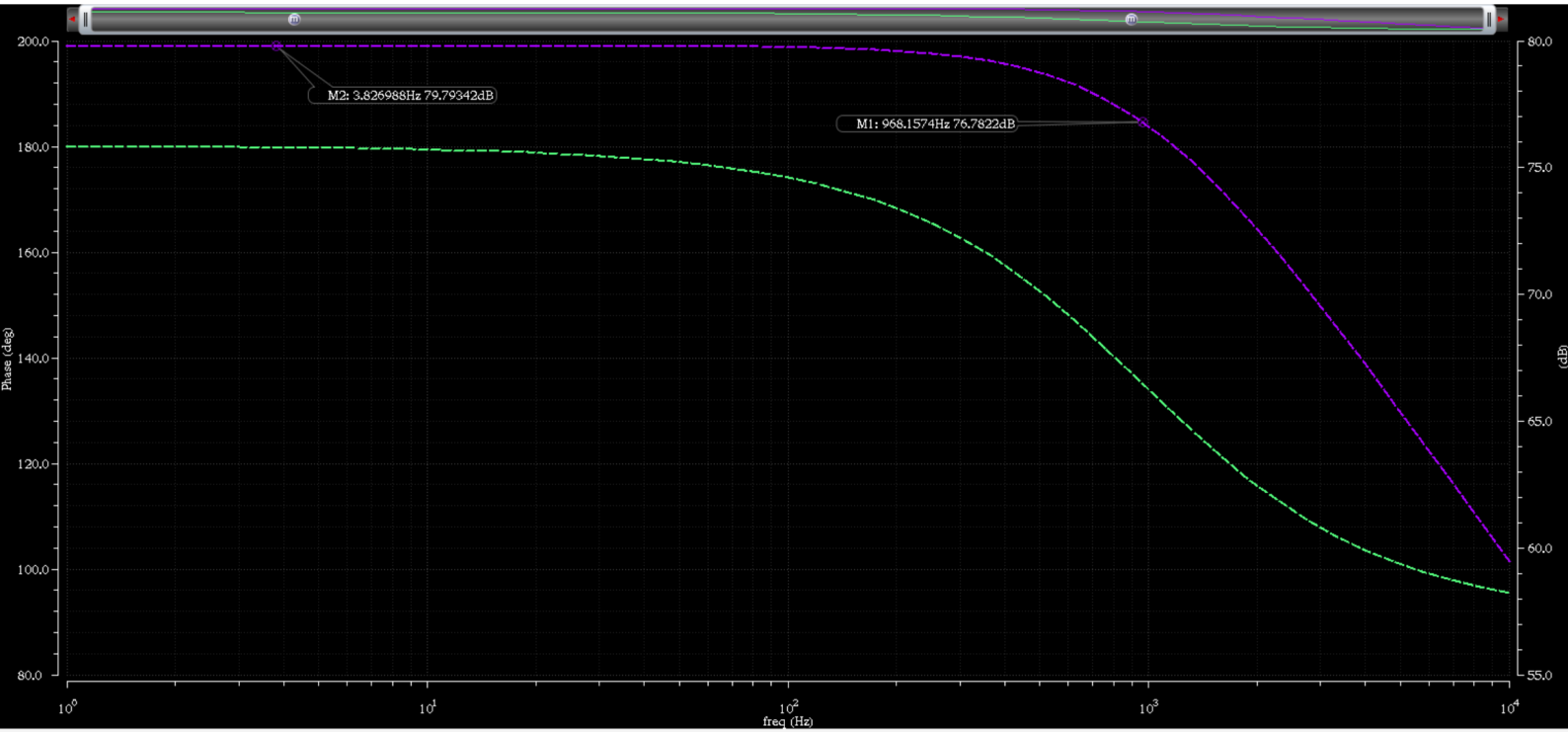
NMOS (Current source) of second stage



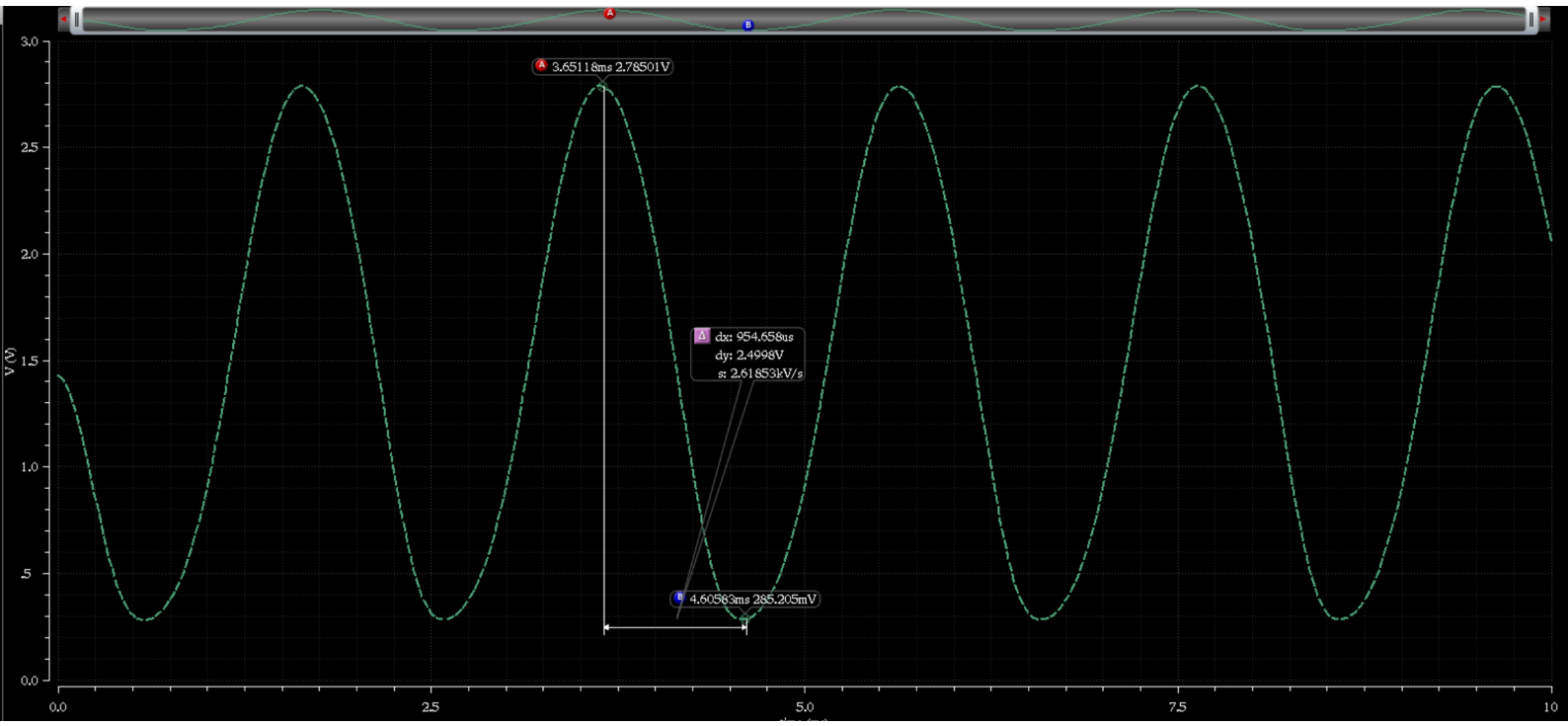
PMOS of second stage

Note: Number of fingers will be selected with layout design.

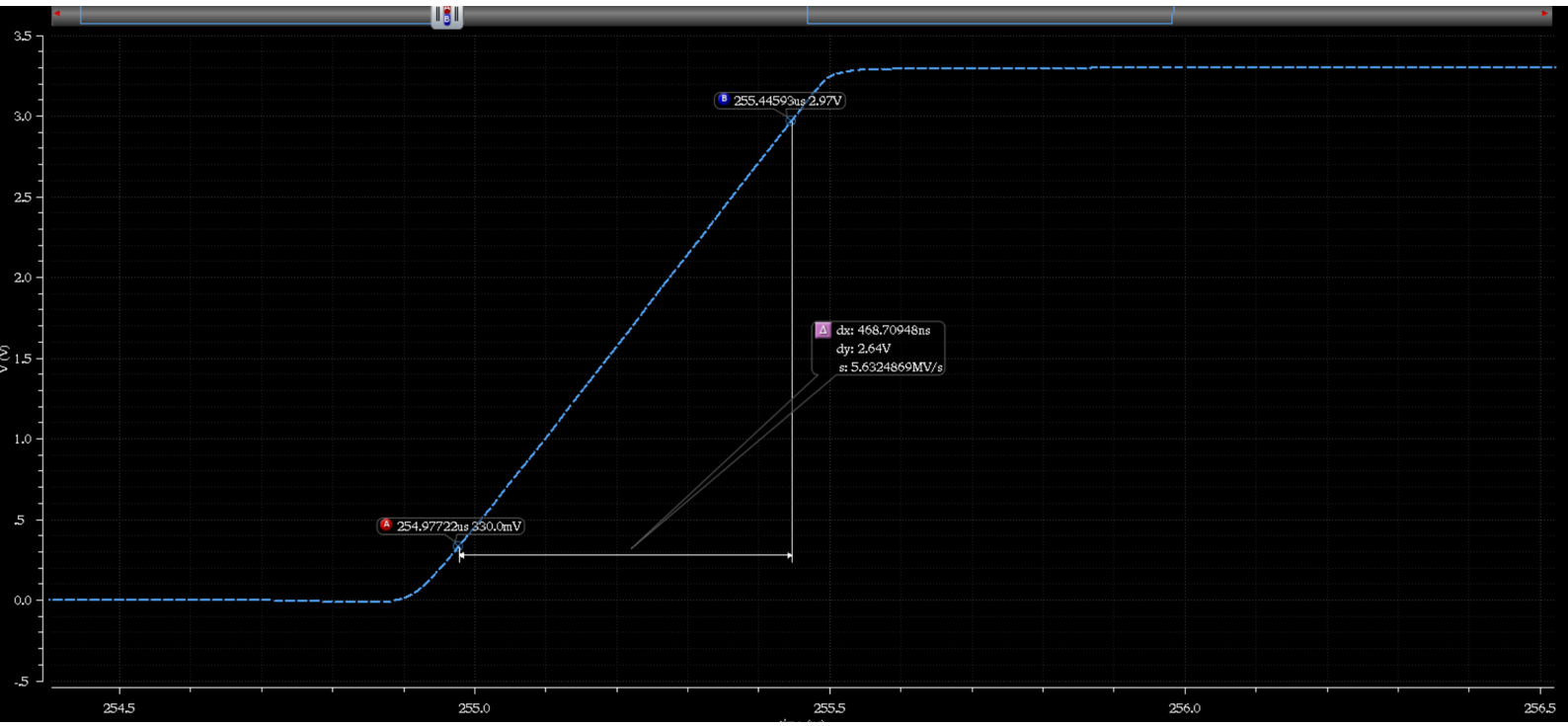
Simulation Results



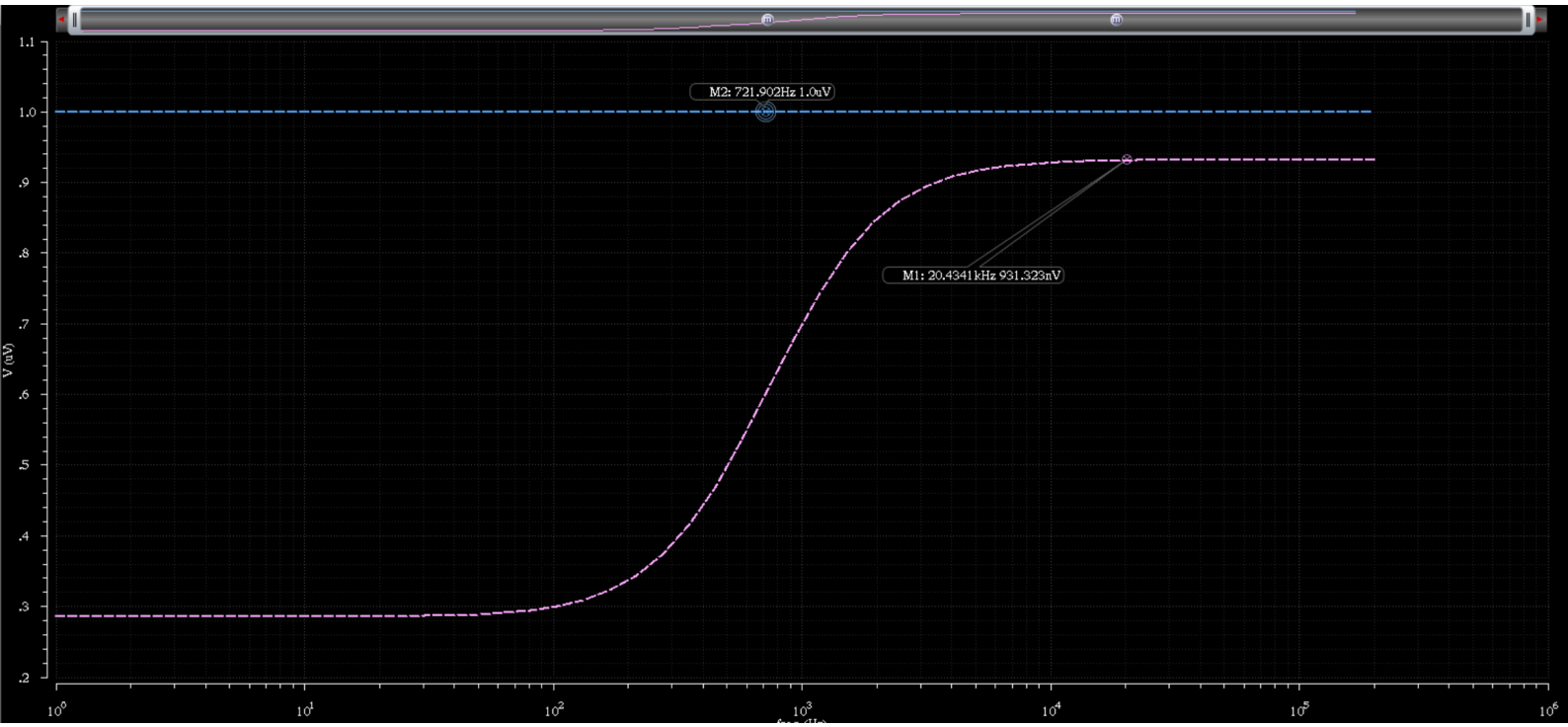
Av ≈ 79.79dB (9764.97), which is slightly lower (~2.35%) than required.
$f_{upper3dB}$ ≈ 968.16 Hz thus Gain Bandwidth ≈ 9.45 MHz, which is lower (~5.46%) then required.



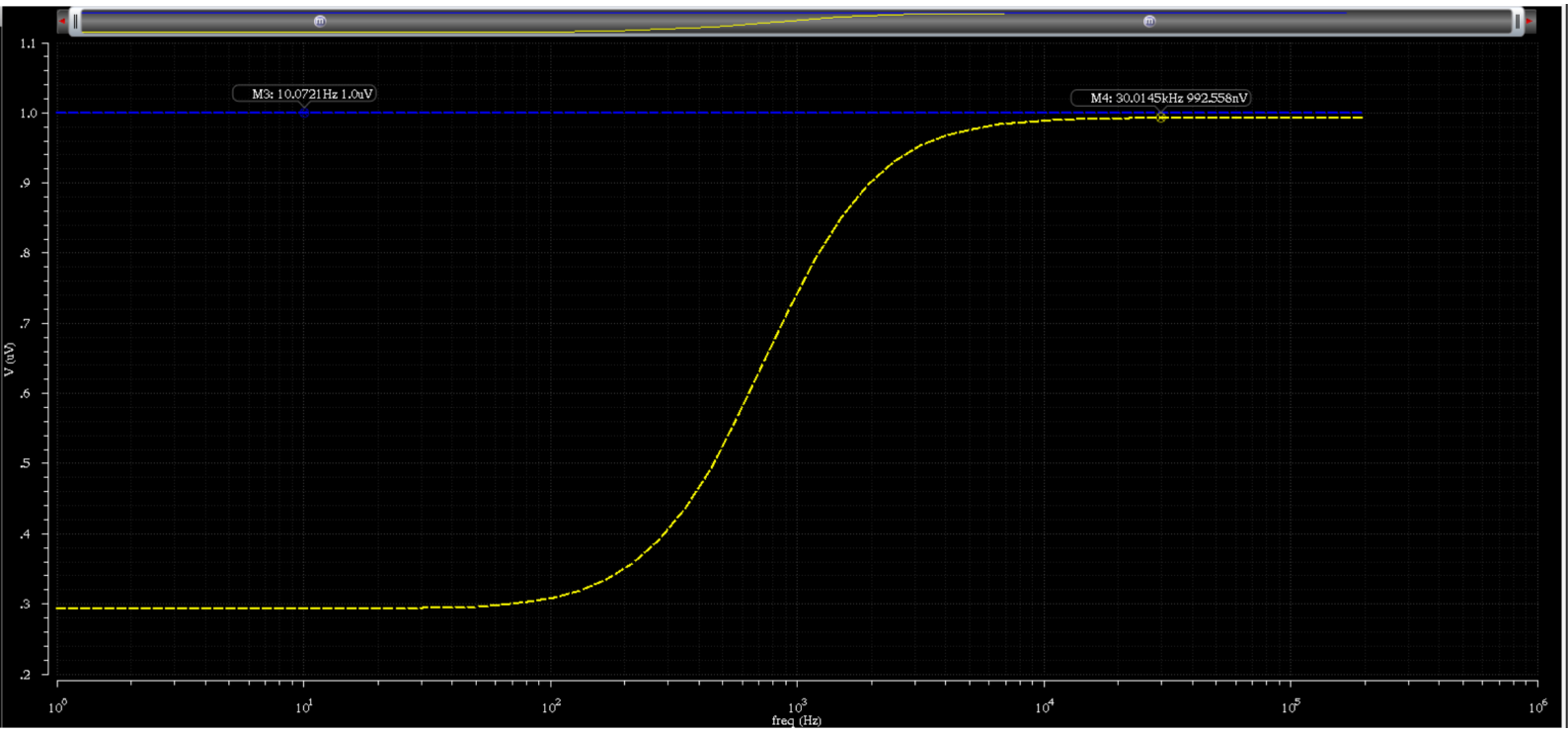
I was able to obtain output voltage swing of ~2.5 V



Slew rate ≈ 5.63 MV/s = 5.63 V/μs as higher (12.6%) than required



By applying small AC voltage to V_{dd} I calculated $PSRR_{dd} = 20*\log(A_v/A_{dd})$
From simulation results $A_{dd} \approx 0.931$ thus $PSRR_{dd} \approx 80.411$ dB



By applying small AC voltage after ground I calculated $PSRR_{ss} = 20*\log(A_v/A_{ss})$
From simulation results $A_{ss} \approx 0.992$ thus $PSRR_{ss} \approx 79.858$ dB
Note: Since our design does not contain V_{ss} I used ground node.

Topology:

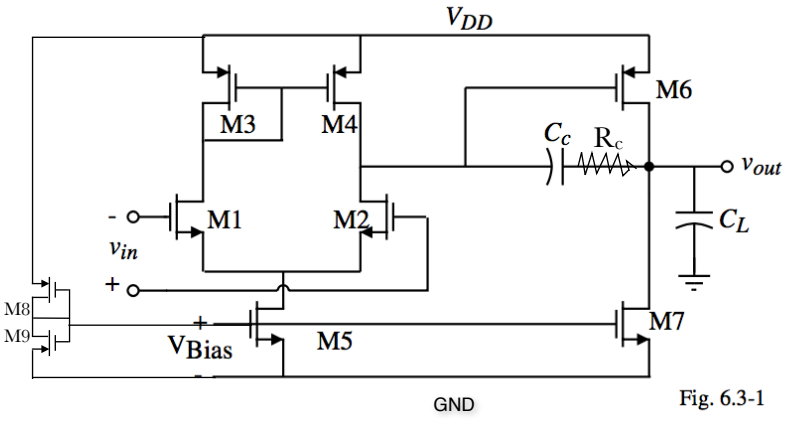


Fig. 6.3-1

My op-amp has three circuits. First one contains M8 and M9 transistors. These transistor are diode connected thus shows ohmic behaviour and used as a voltage divider to provide necessary bias voltage to M5 and M7 transistors (current sources). Second circuit is first stage of op-amp, differential amplifier. Differential stage offers high gain and good noise handling as we see at previous lab assignment. Last circuit is second stage of op-amp, common source amplifier with active current source load. Common source stage provided large output swing.

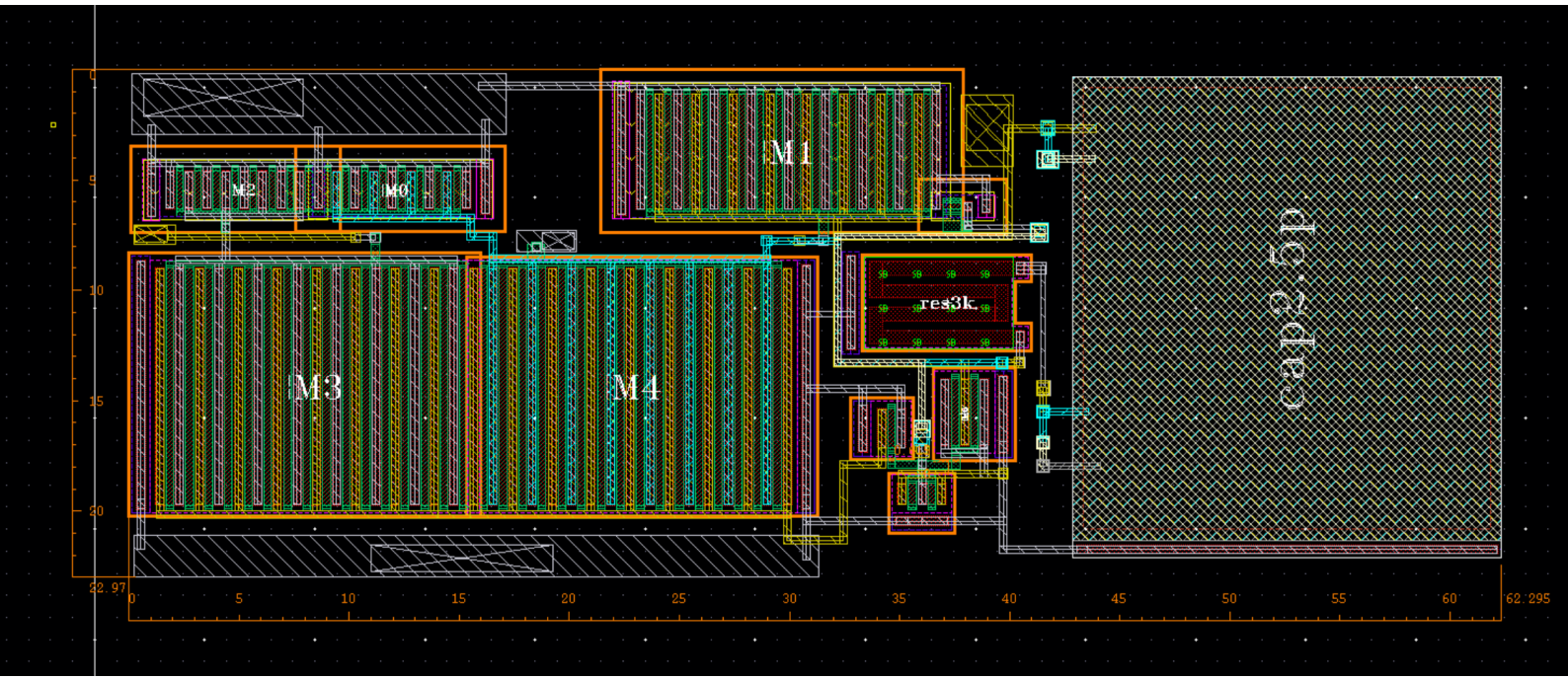
Hand Calculations: (all subscripts refer to Fig. 6.3-1, not schematic)

- I select V_{inDC} = 0.9 V (later decreased it 0.85 V to increase gain)
- I started my calculations with C_c. Since C_L = 10 pF, 0.22 x C_L = 2.2 pF. Thus for PM > 60° C_c > 2.2 pF. I choose C_c = 2.5 pF.
- I calculate I_{5min} = SR x C_c. For SR > 5 V/µs I_5 > 12.5 µA thus $I_4 = I_3$ > 6.25 µA. I choose $I_5 \approx$ 15 µA. (Note that $I_7 >> I_5$)
- For P < 500 µW I_{DDmax} = 151.51 µA. I choose $I_{biascircuit} \approx$ 25 µA thus $I_7 \approx$ 100 µA.
- I calculate W/L ratios of bias transistors using formula $\mu c_{ox}(W/L)V_{gs} = I_d$, equalising I_ds and $V_{Bias} \approx$ 0.9 V. Later I increased L values for lower $I_{biascircuit}$.
- I calculate gm_{1min} from $gm_1 = C_c$ x GBW, gm_1 > 25 µ(Ω^{-1})
- $((W/L)_5/(W/L)_7) = I_5/ I_7 \approx 0.15$
- Later I put my calculations into schematics and simulate. I had to adjust my transistor sizes to increase gain and put $V_{outDC} \approx$ 1.5 V for better voltage swing.

Conclusion (Before layout):

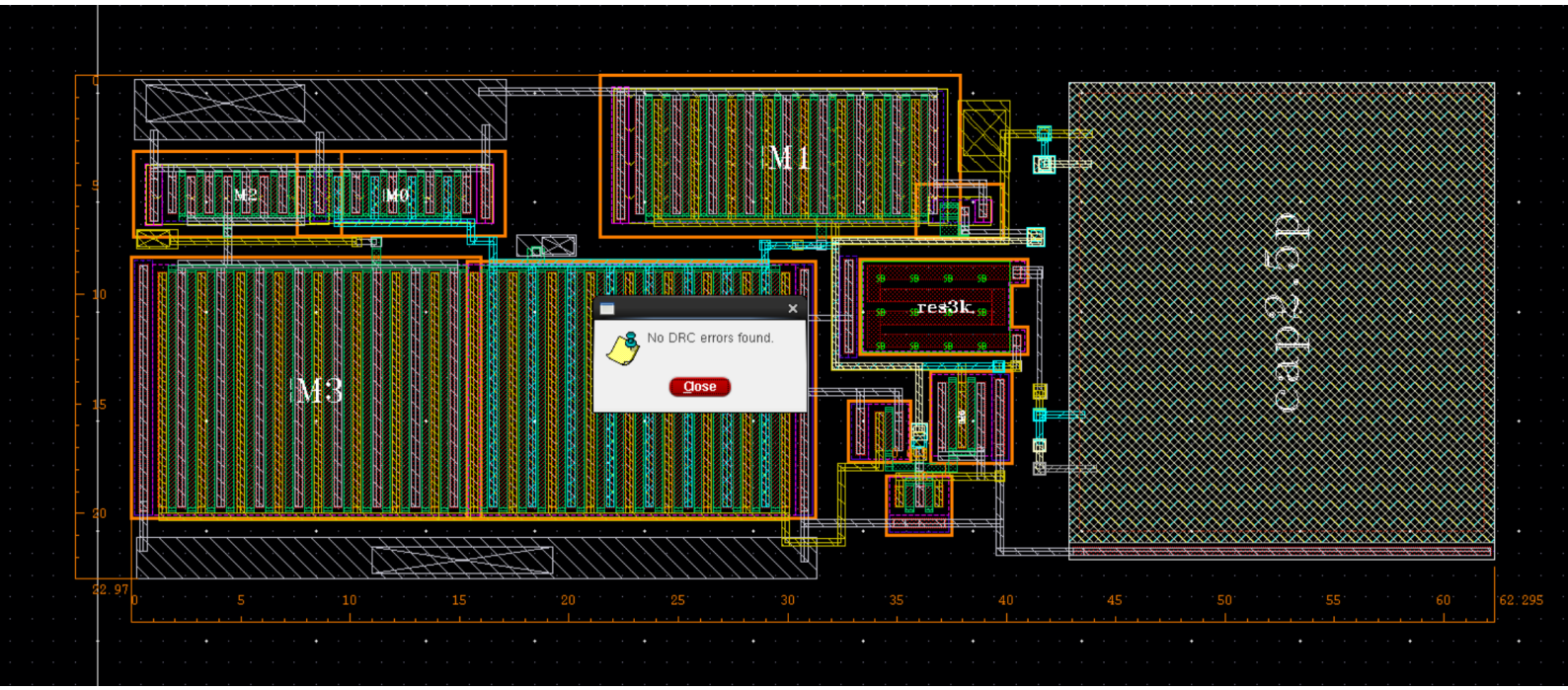
With two stage op-amp we were able to obtain very high gain (~80dB) with bandwidth of ~1kHz. To be able to obtain this much gain, I had to use huge transistors (172µ and 84µ). On the other hand I was able to work with low power (~300 µW) while satisfying Slew rate requirement (~5.6 V/µs). My amplifier provides good power supply rejection ratio for both V_{DD} and V_{SS} (ground) (both ~80dB), if I calculate them correctly. I was able to obtain ~2.5 V voltage swing with a little distortion at minimum value and ~3 V voltage swing with a little distortion at maximum value and some distortion at minimum value (signal is still in sine shape). I had to adjust results of my calculations a lot to get my design working, like previous labs. My initial values and adjusted Width values are different.

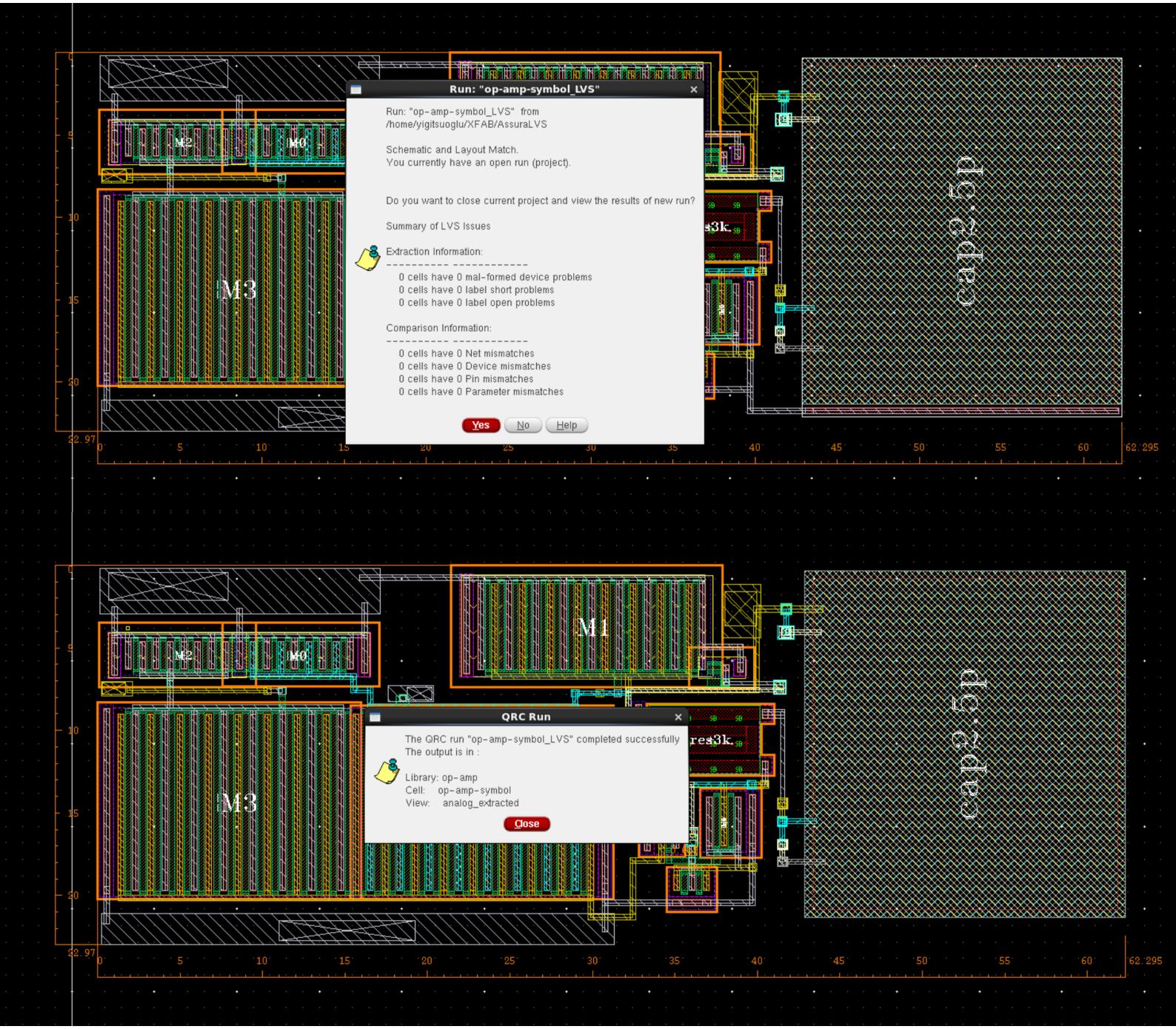
First Layout:



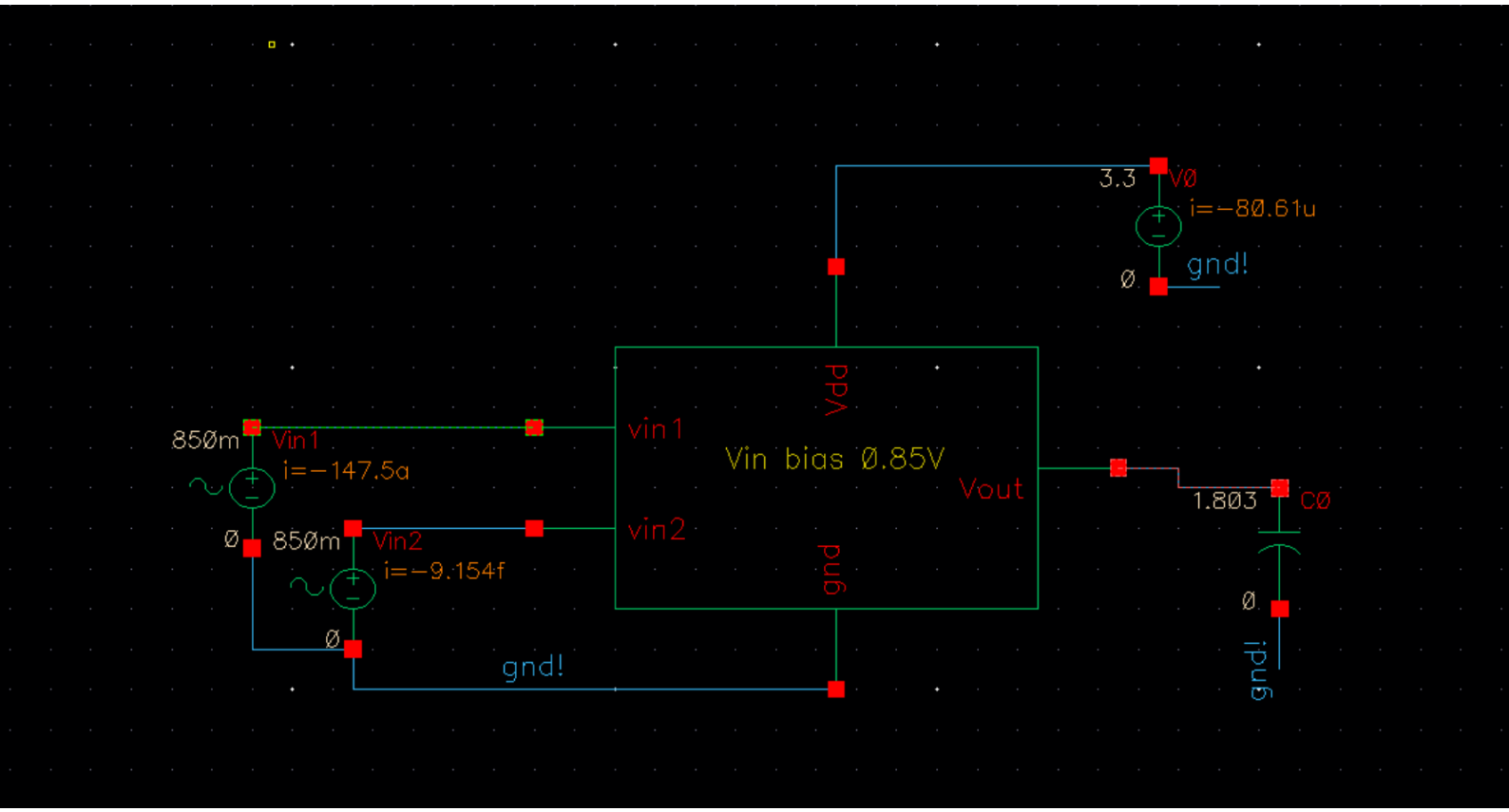
I was able to fit my design in 29.97 x 62.295 rectangle
Note: I change the order of capacitor and resistor

DRC, LVS and QRC (First)



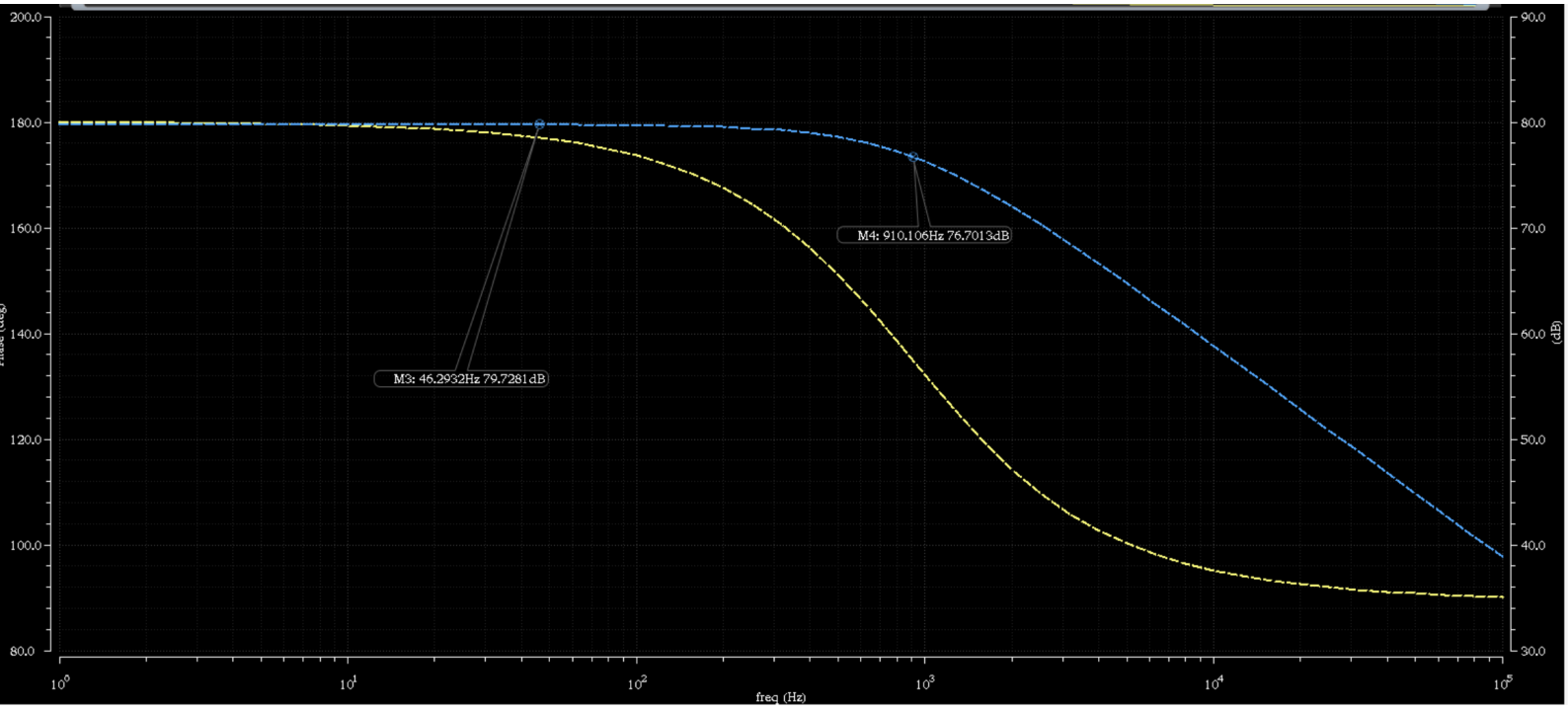

Run: "op-amp-symbol_LVS"
Run: "op-amp-symbol_LVS" from
/home/yigitsuoglu/XFAB/AssuraLVS
Schematic and Layout Match.
You currently have an open run (project).
Do you want to close current project and view the results of new run?
Summary of LVS Issues
Extraction Information:
0 cells have 0 mal-formed device problems
0 cells have 0 label short problems
0 cells have 0 label open problems
Comparison Information:
0 cells have 0 Net mismatches
0 cells have 0 Device mismatches
0 cells have 0 Pin mismatches
0 cells have 0 Parameter mismatches
Yes
No
Help
M2
M0
M3
cap2.5p
QRC Run
The QRC run "op-amp-symbol_LVS" completed successfully
The output is in :
Library: op-amp
Cell: op-amp-symbol
View: analog_extracted
Close
M1

Schematic (After First Layout)



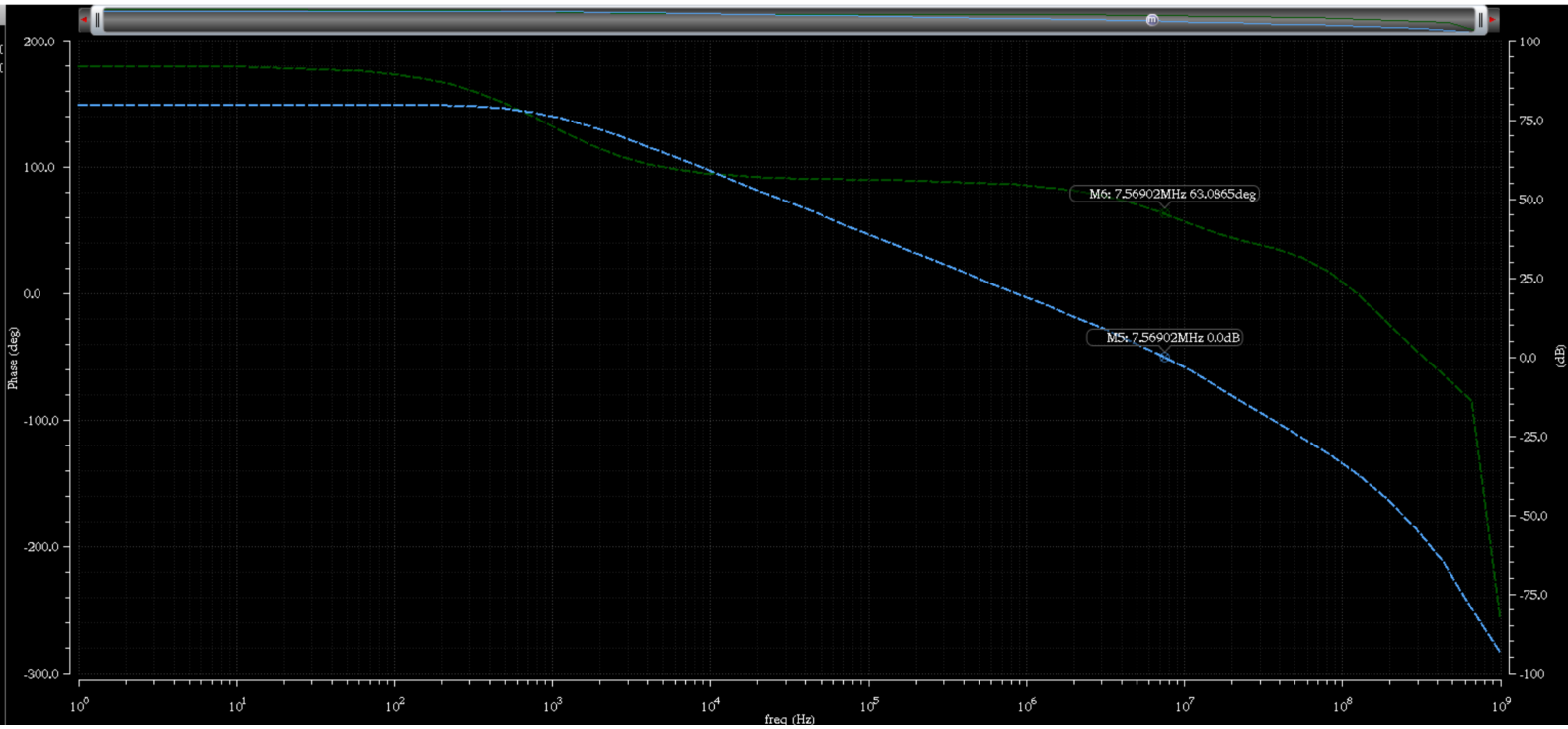
After layout W_{tot} decreased to ~266 µW, nearly half of maximum value
V_{outDC} increased to ~1.8 V

Simulation Results (After First Layout)

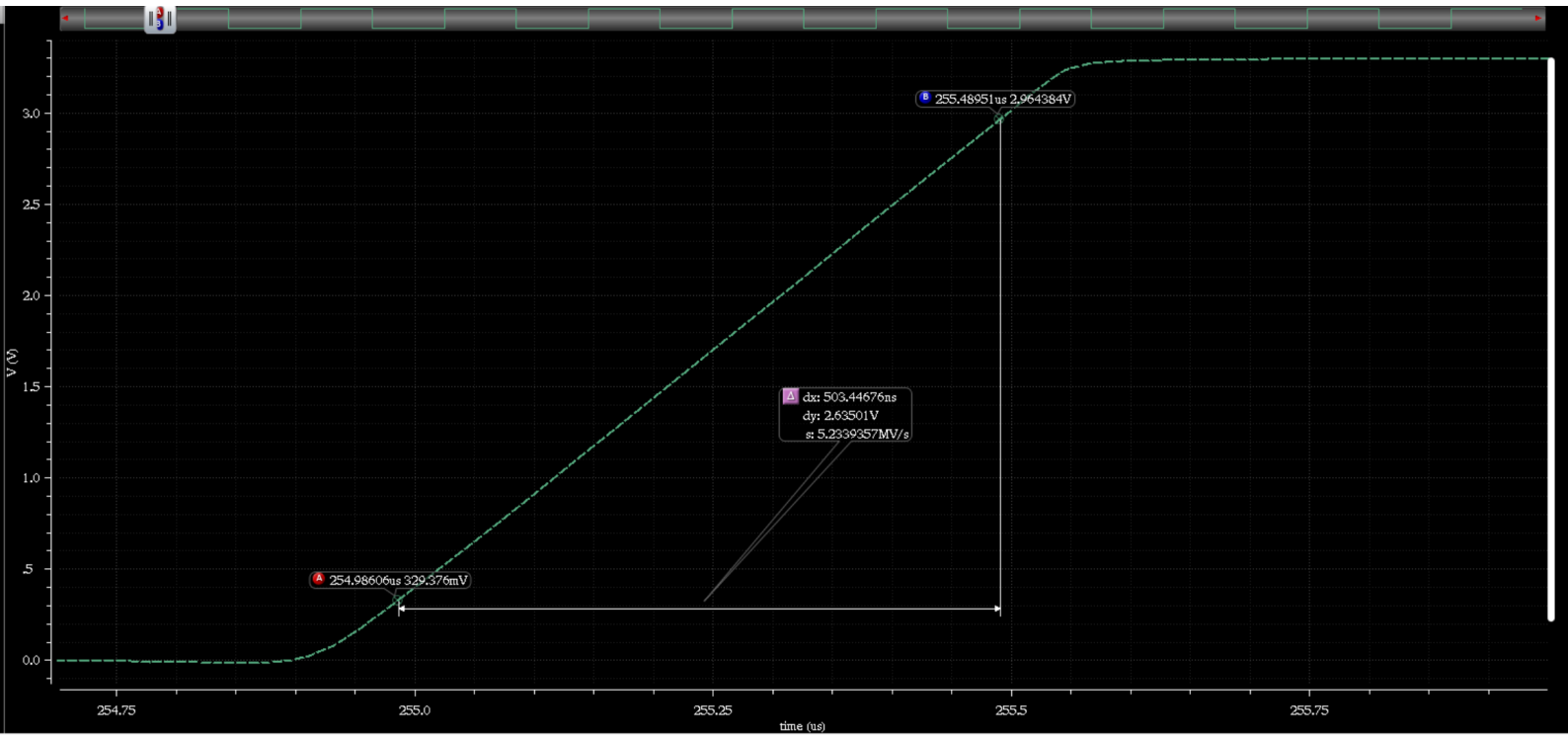


Av decreased to ~79.73 dB, ~ 96939.3 V/V which is ~3% lower than required

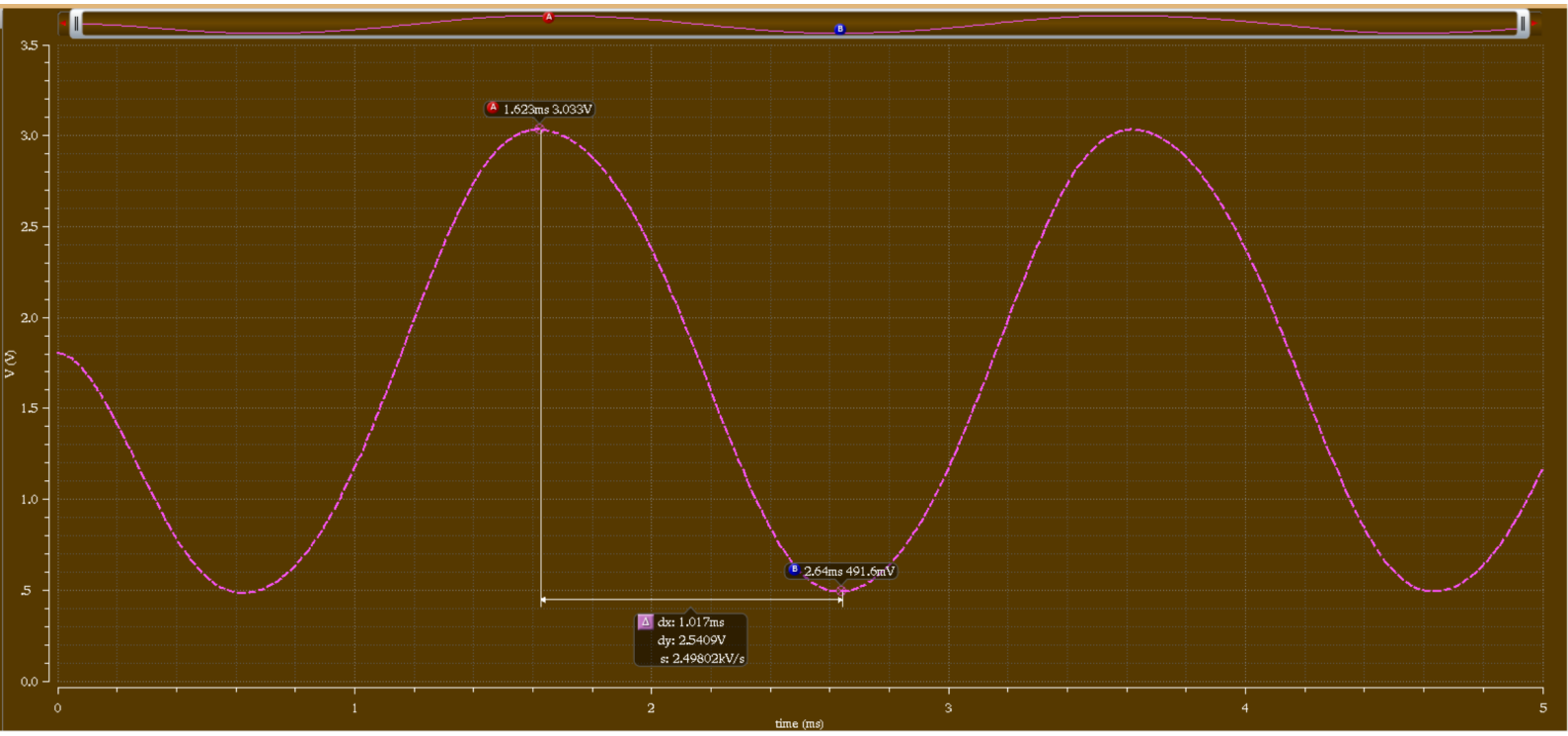
$f_{upper3dB}$ decreased to ~910.1Hz, thus GBW ≈ 8.82MHz ~11.8% lower than required



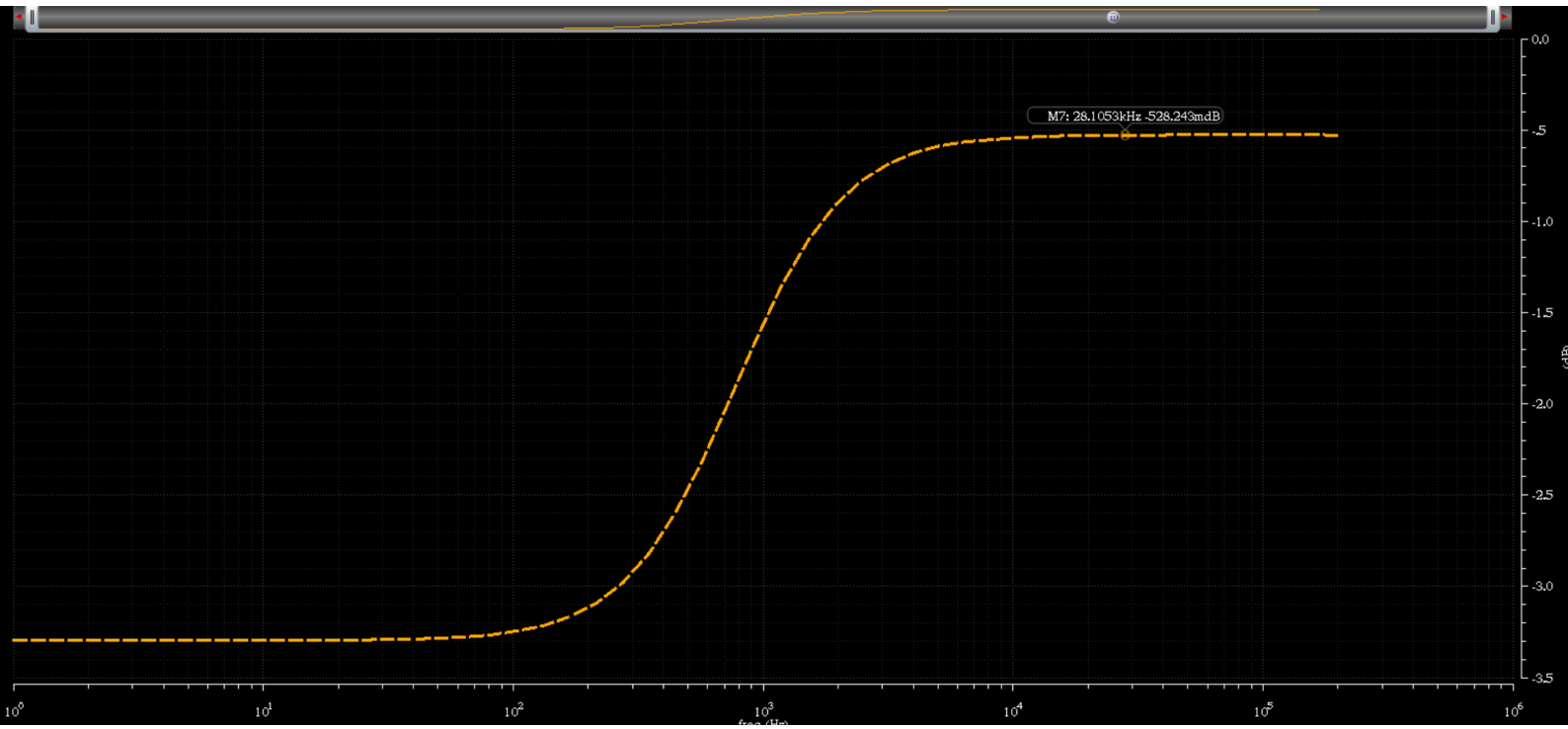
PM = ~63.1 degree as expected



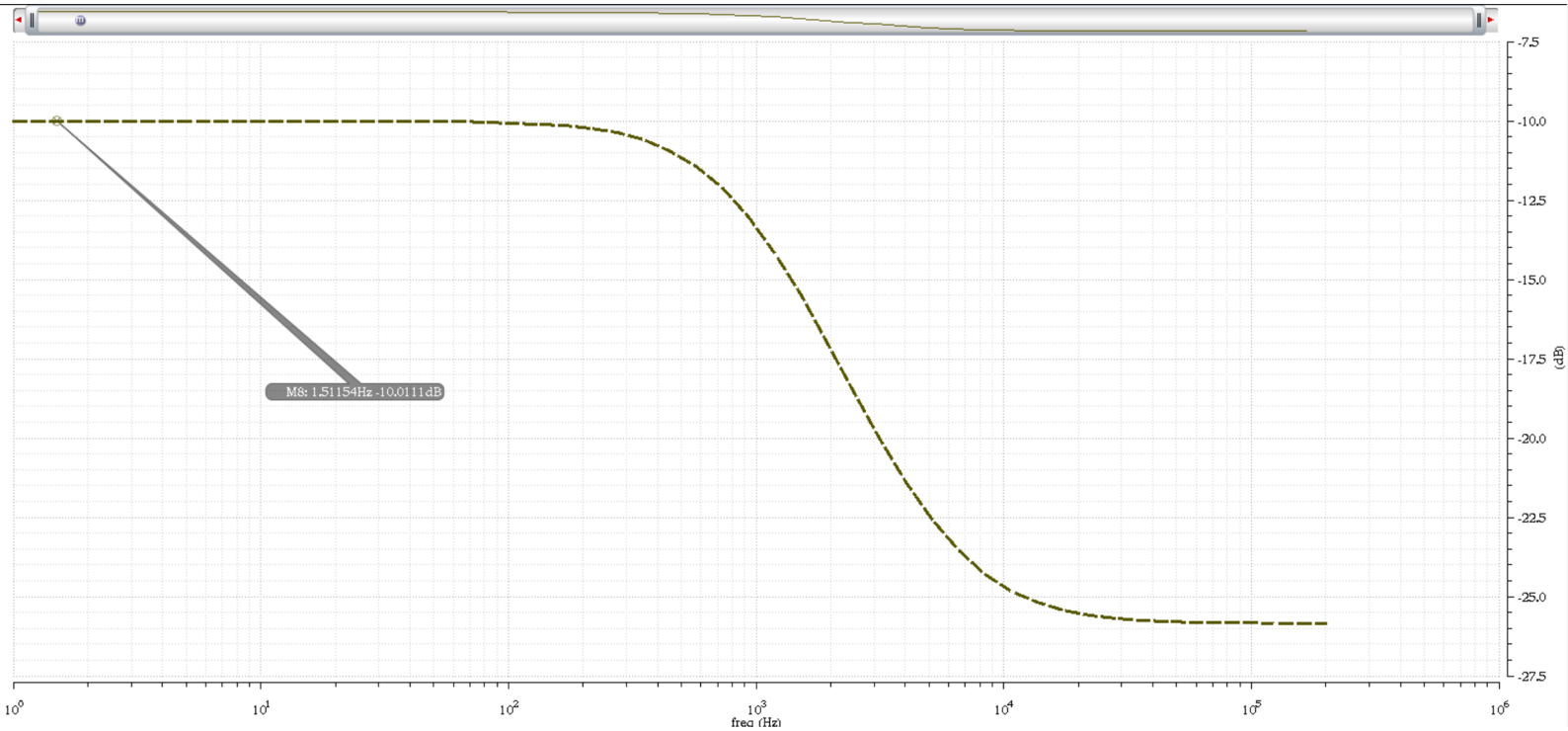
Slew rate decreased to ~5.23 V/µs, still 4.6% higher than required.



I was able to obtain ~2.5V output voltage swing



$A_{dd} \approx$ -0.528 dB thus $PSRR_{Vdd} \approx$ 80.256 dB, more than double of required

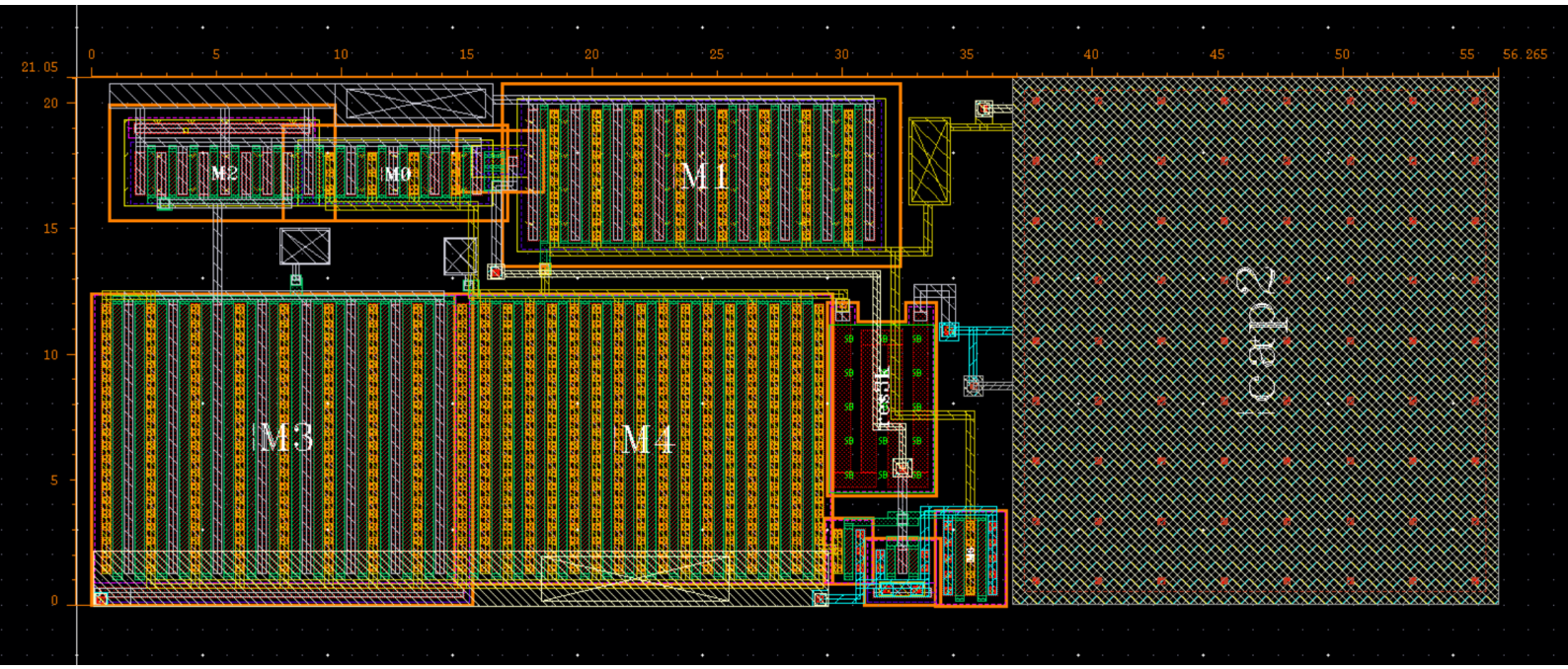


$A_{ss} \approx$ -10.01 dB thus $PSRR_{Vss} \approx$ 89.73 dB, more than double of required

Conclusion (After First Layout):

With two stage op-amp we were able to obtain very high gain (~80dB) with bandwidth of ~900Hz. Size of resulting amplifier is roughly 30 x 62.3. It is huge due to large sized transistors (M1, M3, M4 in layout) and compensation capacitor. Width (62.3 one) can be made smaller by squeezing components between M4 and capacitor. On the other hand my op-amp draws even less current than schematic, resulting $P_{tot} \approx 266$ µW, without violating slew rate requirement (SR ≈ 5.23 V/µs). My op-amp provides even better power supply rejection ratio for both V_{dd} and V_{ss}, ~80dB and ~90dB respectively. Voltage swing (~2.5 V) won't chance between layout and schematic, even through V_{outDC} increased ~0.4V. Between layout and schematic all values are changed. But still only two specifications are not satisfied gain (3% lower) and GBW (~11% lower).

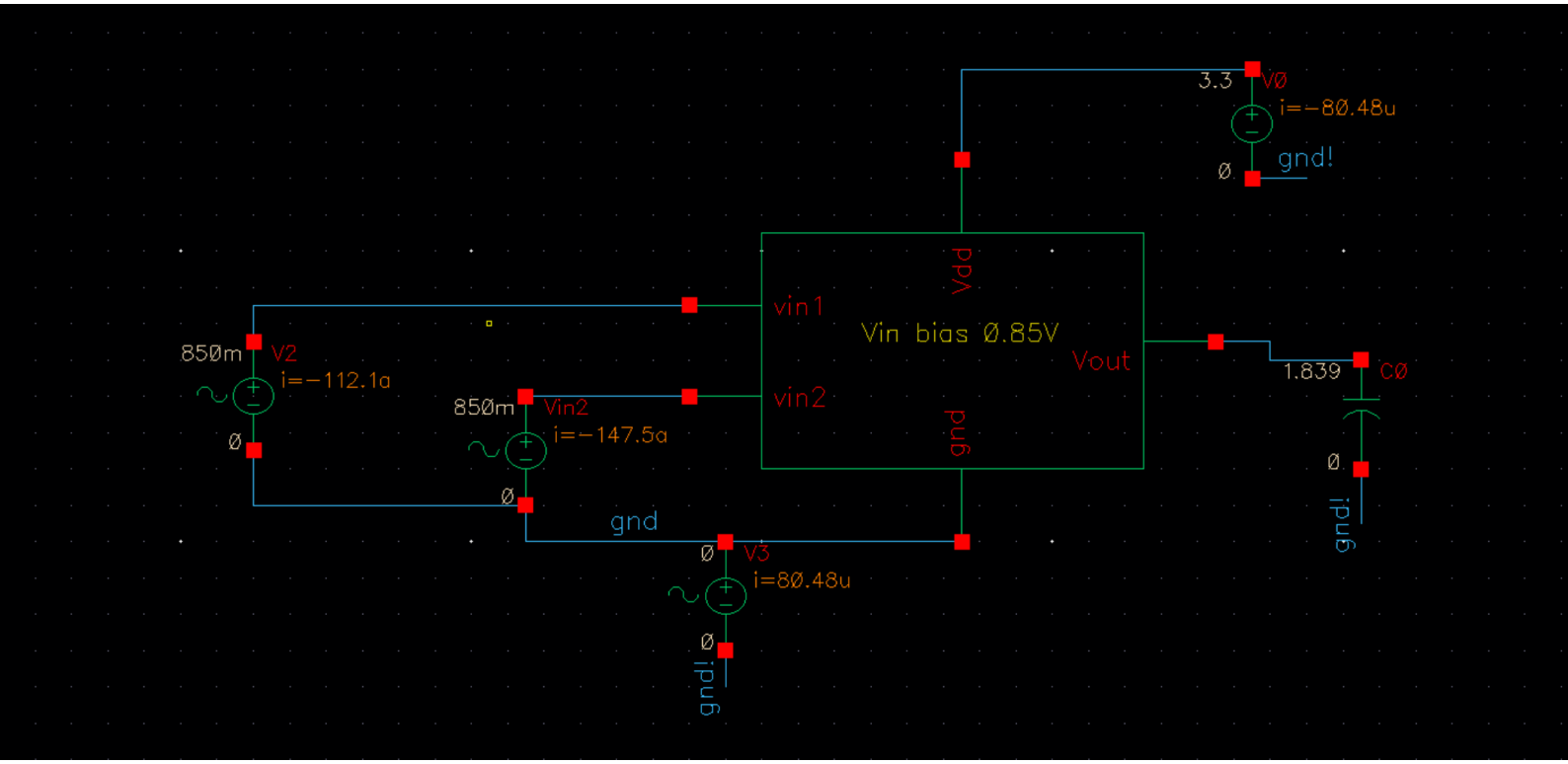
Final Layout



I was able to fit my design in to 21.05 x 56.265 rectangle, ~36.56% smaller than my initial layout.

DRC, LVS and QRC (Final)

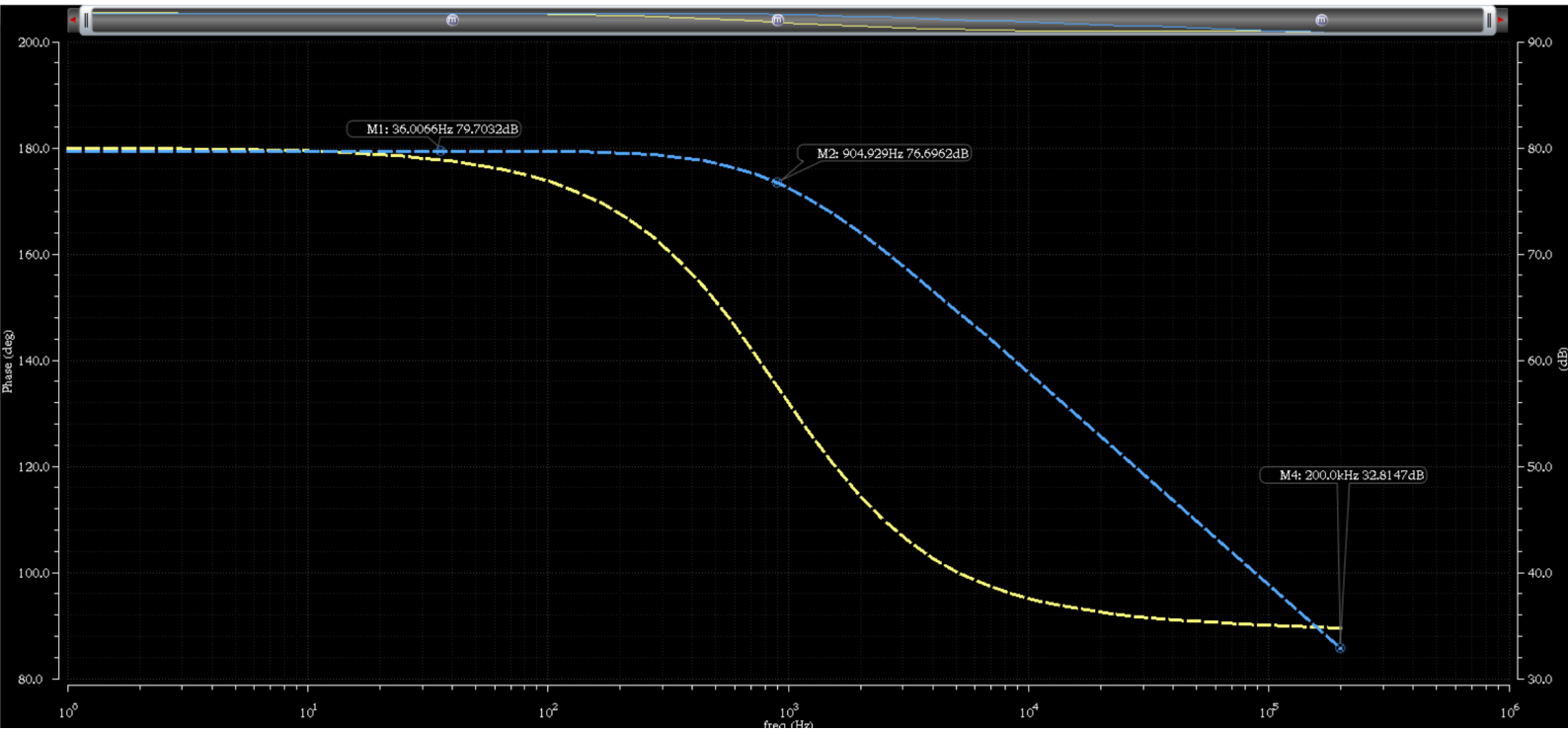
Schematic (Final)



I_{tot} is decreased a little resulting $P_{tot} \approx 265.6\ \mu W$

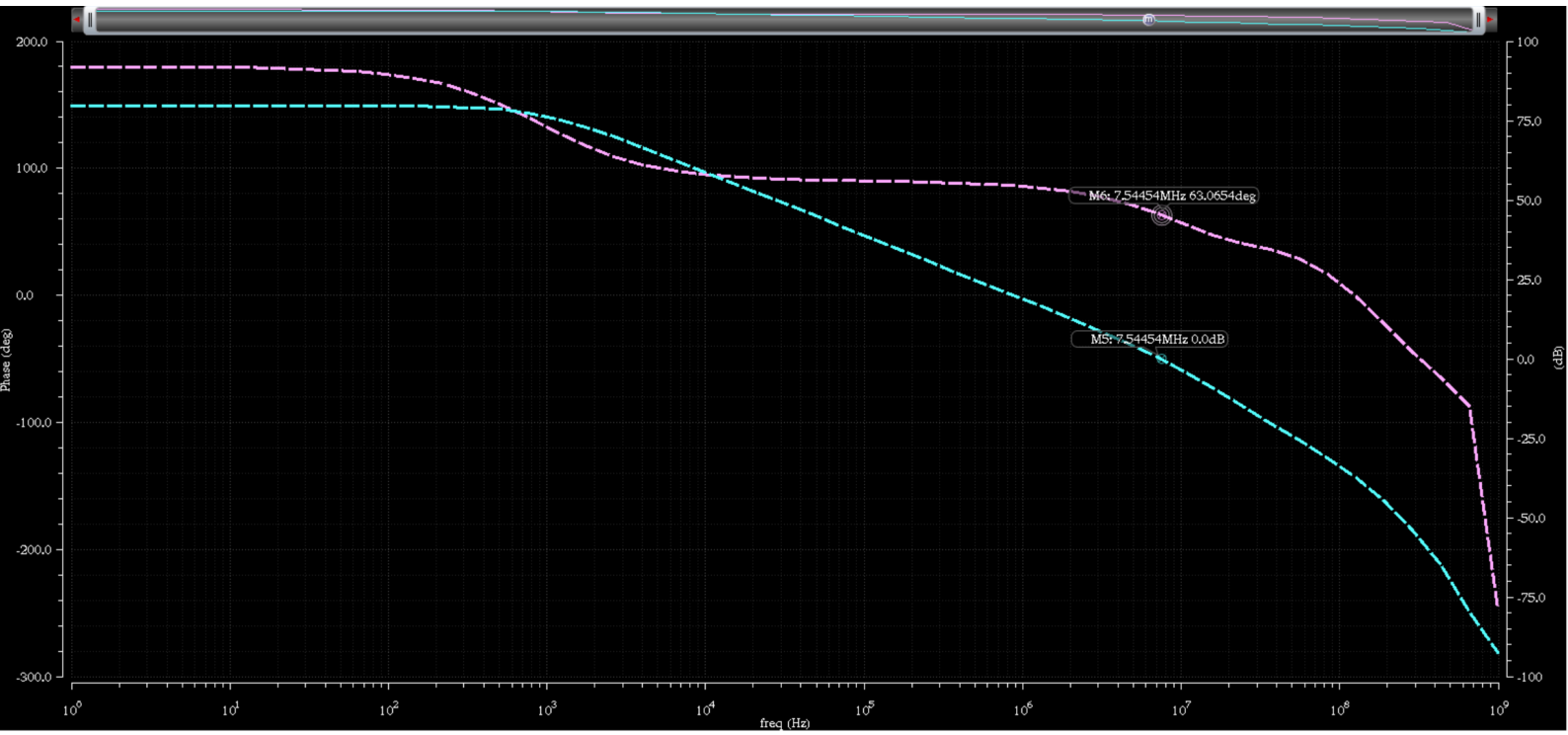
V_{outDC} increased even more, to ~1.84 V

Simulation Results (After First Layout)

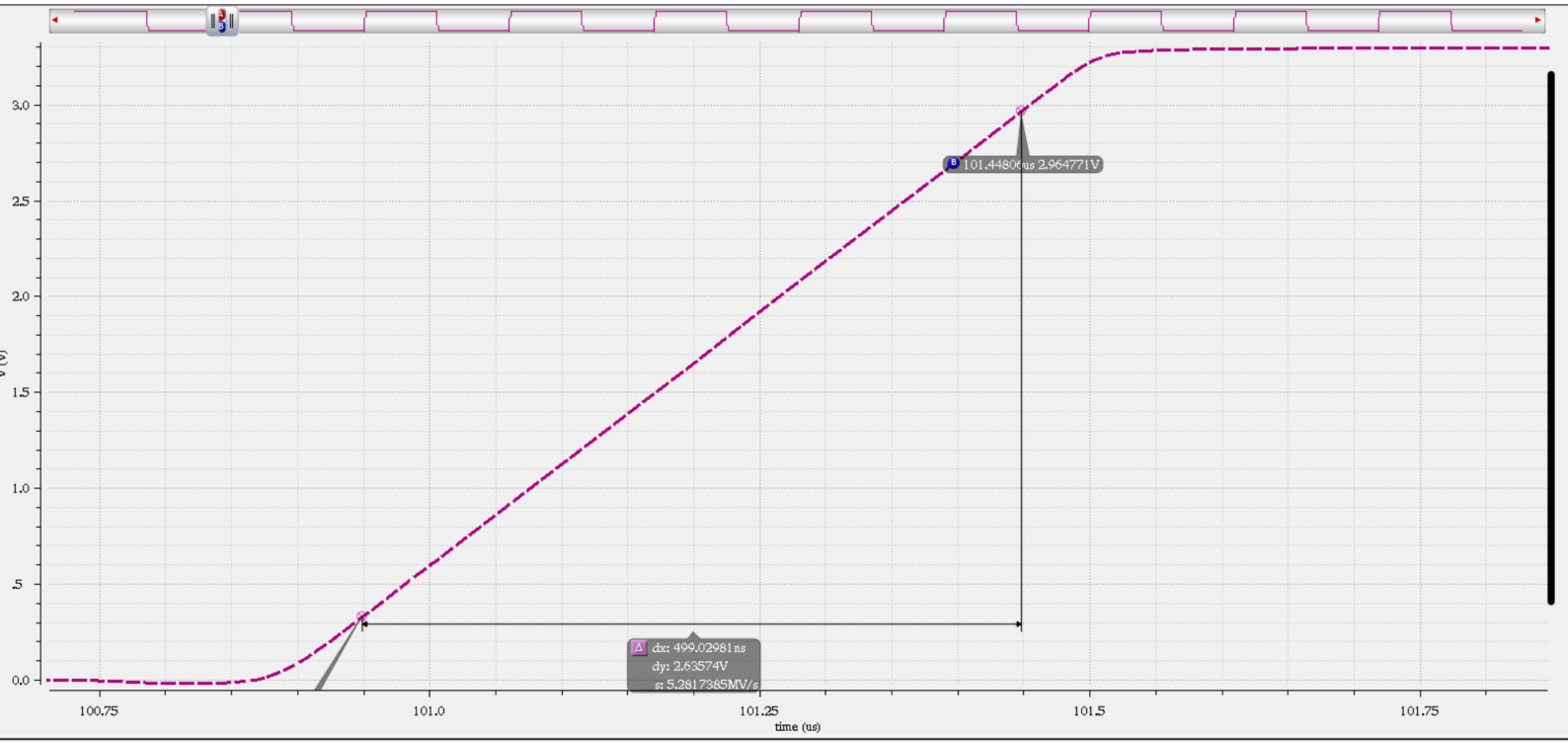


Av decreased even more, to ~79.70 dB, ~ 9660.5 V/V which is ~3.4% lower than required

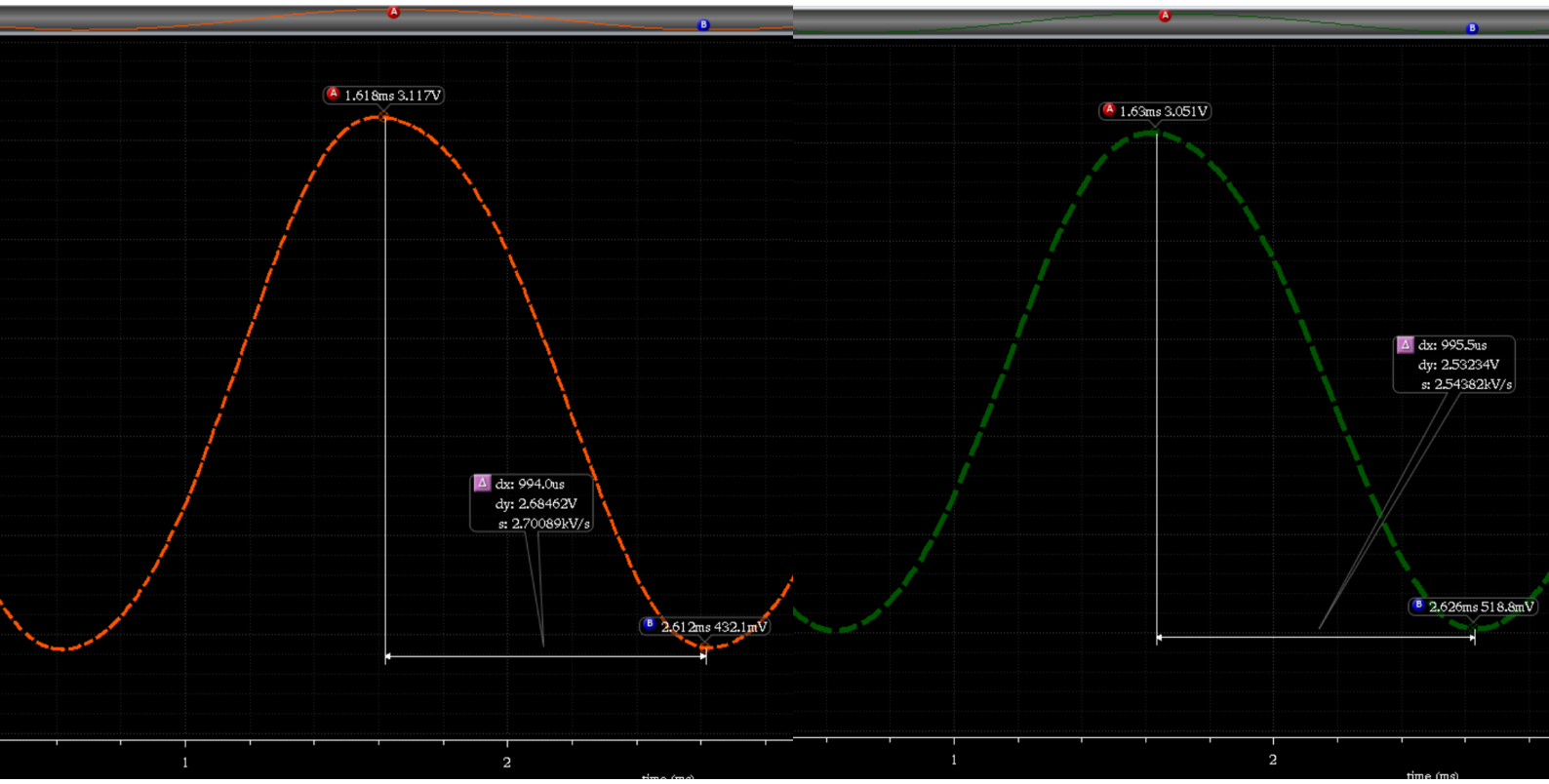
$f_{upper3dB}$ decreased to ~904.9 Hz, thus GBW ≈ 8.74MHz ~12.6% lower than required



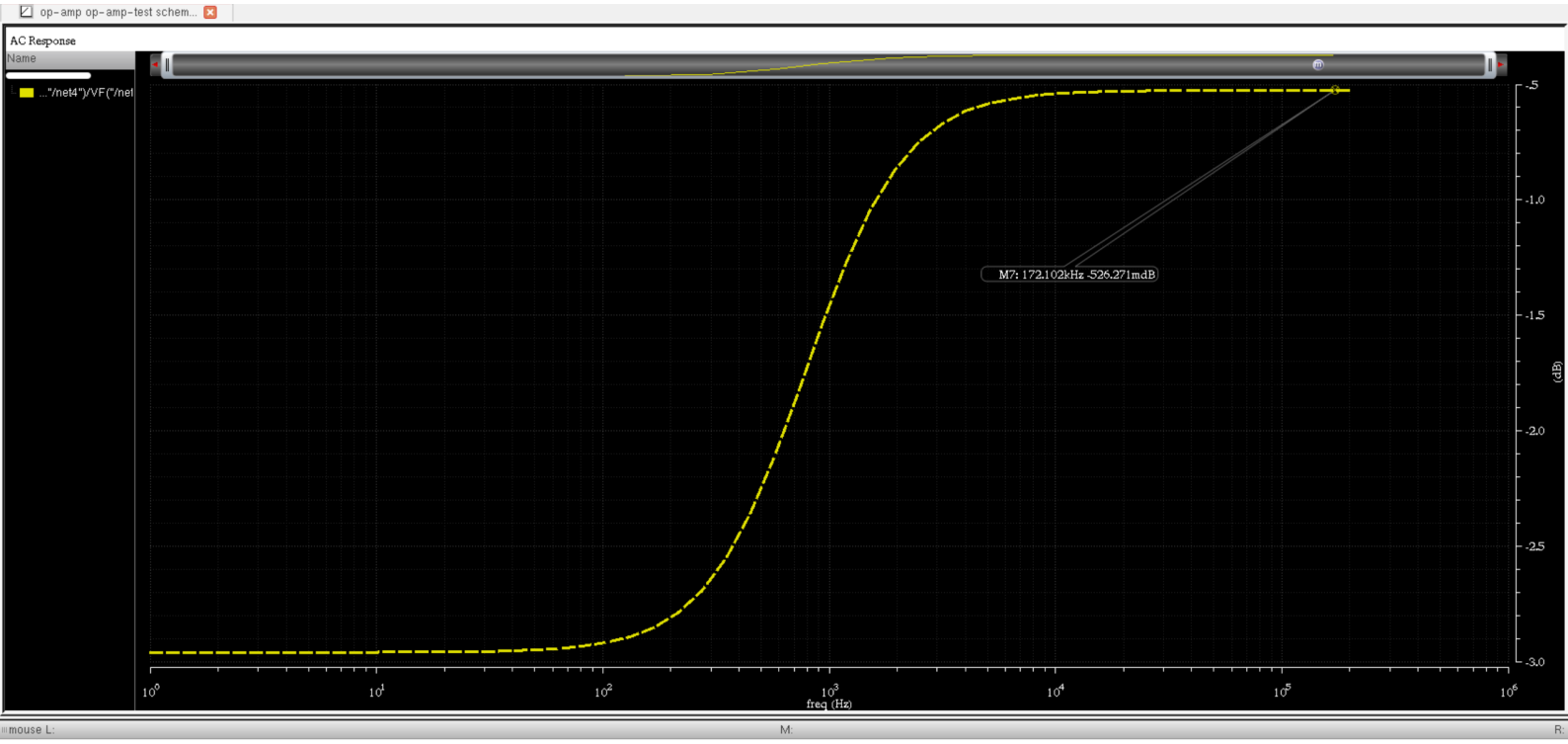
PM ≈ 63.1 deg



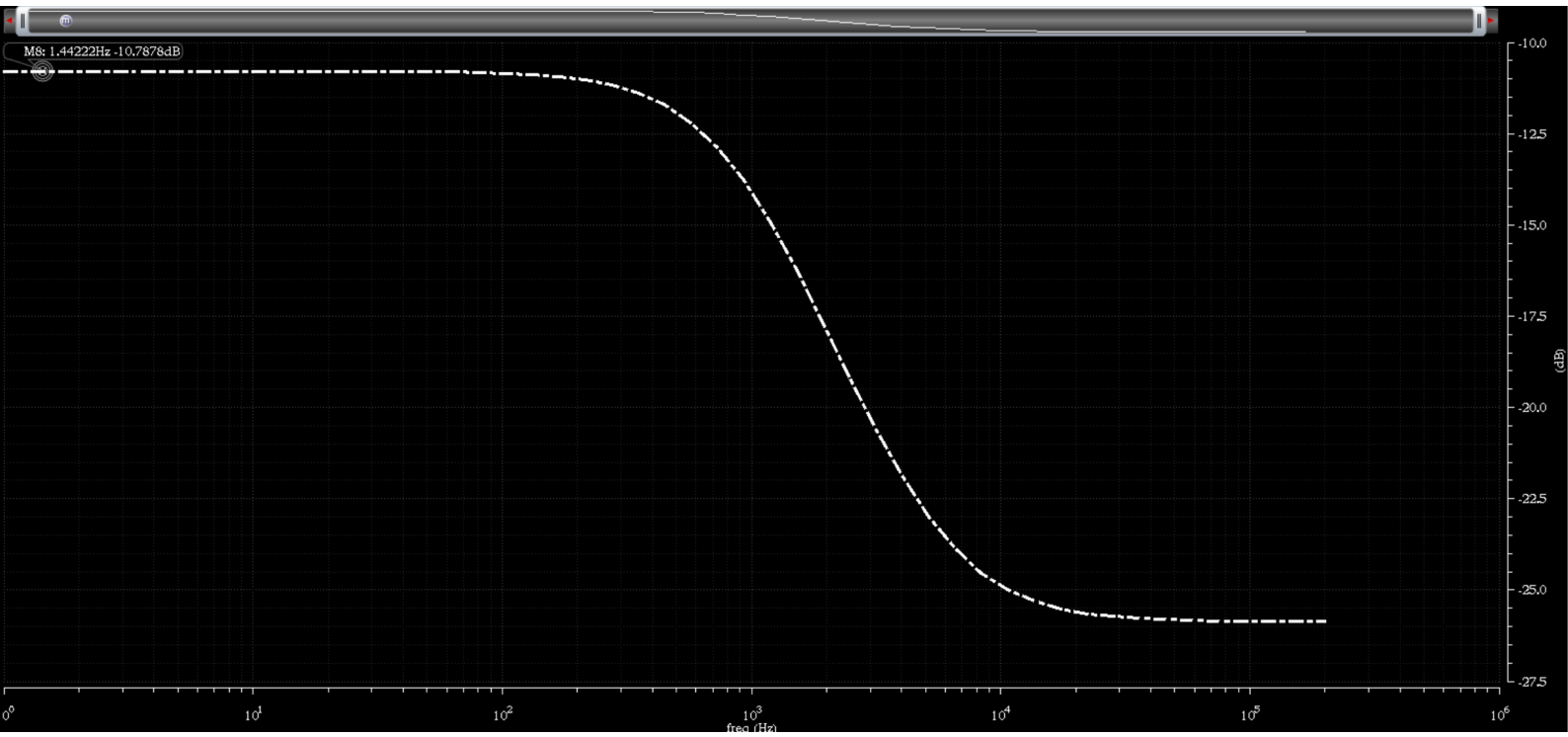
Slew rate ≈ 5.28, increased a little compared to first layout



I was able to obtain ~2.5V output voltage swing



$A_{dd} \approx$ -0.526 dB thus $PSRR_{Vdd} \approx$ 80.229 dB, more than double of required



$A_{ss} \approx$ -10.78 dB thus $PSRR_{Vss} \approx$ 90.49 dB, more than double of required

Conclusion (Final):

I was able to reduce area of my amplifier by 36%, however my gain and gain-bandwidth got worse. My gain is still roughly 3% lower than required and my gain-bandwidth is roughly 13% lower than required, which is too low. I was able to decrease power consumption and increase slew rate at the same time. My PSRR values changed opposite direction, for V_{ss} (ground) increased for V_{dd} decreased. I was able to obtain similar output voltage swing as my first layout.