Two Stage Operational Amplifier

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Yigit Suoglu 17720 Schematic (Before Layout)



 $3.3 \ x \ 89.93 \mu$ = 296.769 $\mu W \approx$ 297 μW much less than 500 μW as required. Cc = 2.5 pF > 2.2 pF = 0.22 x C_{\rm L} thus PM > 60° Also $V_{\rm bias}$ = 899.9 mV \approx 0.9 V

Transistor Properties

Library Name PR	IMLIB	off 🔽	Library Name PF	RIMLIB
Cell Name ne	3	value 🔽	Cell Name pe	e3
View Name sy	mbol	off 🔽	View Name sy	ymbol
Instance Name 117	biasDown	off 🔽	Instance Name	biasUP
	Add Delete Modify	\supset		Add Delete Modify
CDF Parameter	Value	Display	CDF Parameter	Value
lodel name	ne3	off 🔽	Model name	pe3
/oltage	3.6	off 🧧	Voltage	3.6
Calculate Width Method	FingerWidth DeviceWidth	off 🔽	Calculate Width Method	🔾 FingerWidth 🥑 DeviceWidth
Aodel Limits	⊻	off 🔽	Model Limits	⊻
Device Width	2u M	off 🔽	Device Width	300n M
/idth per Finger	2u M	off 🔽	Width per Finger	300n M
ength	360.0n M	off 🔽	Length	800n M
umber of Fingers	1	off 🔽	Number of Fingers	1
fultiplier	1	off 🔽	Multiplier	1
for Simulators	<pre>iPar("m")*iPar("ng")</pre>	off 🔽	m for Simulators	<pre>iPar("m")*iPar("ng")</pre>
alculation Method	edit parasitics & callbacks off 🔽	off 🔽	Calculation Method	callbacks enabled
)rain diffusion area	2.4e-13	off 🔽	Drain diffusion area	1.44e-13
iource diffusion area	2.4e-13	off 🔽	Source diffusion area	1.44e-13
rain diffusion periphery	1.96e-06	off 🔽	Drain diffusion periphery	1.56e-06
ource diffusion periphery	1.96e-06	off 🔽	Source diffusion periphery	1.56e-06
rain diffusion res squares	0.54	off 🔽	Drain diffusion res squares	0.9
ource diffusion res squares	0.54	off 🔽	Source diffusion res squares	0.9
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Property	Value	Display	Library Name	PRIMLIB	off
Library Name	PRTMLTB	off	Cell Name	pe3	value
Cell Name	~~?	value	View Name	symbol	off
View Neme			Instance Name	٠ ١٣	off
view Name	symbol				
Instance Name	МЗ			Add Delete Modify	
	Add Delete Modify		CDF Parameter	Value	Displa
CDF Parameter	Value	Display	Model name	pe3	off
vlodel name	ne3	off 🔽	Voltage	3.6	off
/oltage	3.6	off 🔽	Calculate Width Method	FingerWidth DeviceWidth	off
Calculate Width Method	FingerWidth DeviceWidth	off 🔽	Model Limits	⊻	off
Model Limits	⊻	off 🔽	Device Width	14.0u M	off
Device Width	172.000000u M	off 🔽	Width per Finger	14.0u M	off
Vidth per Finger	172.000000u M	off 🔽	Length	300n M	off
ength	350.0n M	off 🔽	Number of Fingers	1	off
Number of Fingers	1	off 🔽	Multiplier	1	off
∕lultiplier	1	off 🔽	m for Simulators	<pre>iPar("m")*iPar("ng")</pre>	off
n for Simulators	<pre>iPar("m")*iPar("ng")</pre>	off 🔽	Calculation Method	callbacks enabled	off
Calculation Method	callbacks enabled	off 🔽	Drain diffusion area	6.72e-12	off
Drain diffusion area	8.256e-11	off 🔽	Source diffusion eree	6.726-12	off
Source diffusion area	8.256e-11	off 🔽	Droin diffusion parinharu	0.000-05	off
Drain diffusion periphery	0.00034496	off 🔽	Drain uniusion periphery	2.0966-05	off
Source diffusion periphery	0.00034496	off 🔽	Source aimusion periphery	2.8968-05	
Drain diffusion res squares	0.00156977	off 🔽	Drain diffusion res squares	0.0192857	σπ
Source diffusion res squares	0.00156977	off 🔽	Source diffusion res squares	0.0192857	off
				1011	



Current Source of first stage

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Browse	Reset Instance Labels Display		Property	Value	Di
Property	Value	Display	Library Name	PRIMLIB	off
Library Name	PRIMLIB	off 🔽	Cell Name	pe3	valu
Cell Name	ne3	value 🔽	View Name	symbol	off
View Name	symbol	off 🔽	Instance Name	MI	off
Instance Name	M6	off 🔽		Add Delete Modify	_
	Add Delete Modify		CDE Parameter	Value	Di
CDF Parameter	Value	Display	Model name	Value	off
Model name	ne3	off 🔽	Voltane	3.6	off
Voltage	3.6	off 🔽 🔳	Calculate Width Method	O FingerWidth ● DeviceWidth	off
Calculate Width Method	FingerWidth I DeviceWidth	off 🔽	Model Limite		off
/lodel Limits	V	off 🔽	Device Width	■	off
Device Width	6u M	off 🔽	Device width	84.0u M	off
Vidth per Finger	6u M	off 🔽	wiath per Finger	84.UU M	UII off
ength	350.0n M	off 🔽	Length	300n M	01
lumber of Fingers	1	off 🔽	Number of Fingers	1	σπ
Aultiplier	1	off 🔽	Multiplier	1	off
1 for Simulators	<pre>iPar("m")*iPar("ng")</pre>	off 🔽	m for Simulators	iPar("m")*iPar("ng")	off
alculation Method	callbacks enabled	off	Calculation Method	callbacks enabled	off
)rain diffusion area	2 88e-12	off	Drain diffusion area	4.032e-11	off
ource diffusion area	2.000-12	off	Source diffusion area	4.032e-11	off
)rain diffusion paripharu	1 2060 05		Drain diffusion periphery	0.00016896	off
Source diffusion periphery	1.2968-05		Source diffusion periphery	0.00016896	off
ource amusion periphery	1.2908-05		Drain diffusion res squares	0.00321429	off
oram umusion res squares	0.045		Source diffusion res square	s 0.00321429	off
source diffusion res squares	0.045				

NMOS (Current source) of second stage

PMOS of second stage

Note: Number of fingers will be selected with layout design.

Simulation Results



$$\label{eq:Av} \begin{split} Av &\approx 79.79 dB~(9764.97) \text{, which is slightly lower}~(\sim 2.35\%) \text{ than required.} \\ f_{upper3dB} &\approx 968.16~Hz \text{ thus Gain Bandwidth} \approx 9.45~MHz \text{, which is lower}~(\sim 5.46\%) \text{ then required.} \end{split}$$



I was able to obtain output voltage swing of ~ 2.5 V



Slew rate ≈ 5.63 MV/s = 5.63 V/µs as higher (12.6%) than required



By applying small AC voltage to $V_{dd}I$ calculated $PSRR_{dd}$ = 20*log(A_v/A_{dd}) From simulation results $A_{dd} \approx 0.931$ thus $PSRR_{dd} \approx 80.411~dB$



By applying small AC voltage after ground I calculated PSRR_{ss} = $20*\log(A_v/A_{ss})$ From simulation results $A_{ss} \approx 0.992$ thus PSRR_{ss} ≈ 79.858 dB Note: Since our design does not contain V_{ss} I used ground node.



My op-amp has three circuits. First one contains M8 and M9 transistors. These transistor are diode connected thus shows ohmic behaviour and used as a voltage divider to provide necessary bias voltage to M5 and M7 transistors (current sources). Second circuit is first stage of op-amp, differential amplifier. Differential stage offers high gain and good noise handling as we see at previous lab assignment. Last circuit is second stage of op-amp, common source amplifier with active current source load. Common source stage provided large output swing.

Hand Calculations: (all subscripts refer to Fig. 6.3-1, not schematic)

- I select $V_{inDC} = 0.9 V$ (later decreased it 0.85 V to increase gain)
- I started my calculations with C_c. Since C_L = 10 pF, 0.22 x C_L = 2.2 pF. Thus for PM > 60° C_c > 2.2 pF. I choose C_c = 2.5 pF.
- I calculate I_{5min} = SR x C_c. For SR > 5 V/µs I_5 > 12.5 µA thus I_4 = I_3 > 6.25 µA. I choose $I_5 \approx$ 15 µA. (Note that I_7 >> I_5)
- For P < 500 μ W I_{DDmax} = 151.51 μ A. I choose I_{biascircuit} \approx 25 μ A thus I₇ \approx 100 μ A.
- I calculate W/L ratios of bias transistors using formula $\mu c_{ox}(W/L)V_{gs}$ = I_d, equalising I_{ds} and V_{Bias} \approx 0.9 V. Later I increased L values for lower I_{biascircuit}.
- + I calculate gm_{1min} from gm_1 = $C_c \ x$ GBW, $gm_1 > 25 \ \mu(\Omega^{\text{-}1})$
- $((W/L)_5/(W/L)_7) = I_5/I_7 \approx 0.15$
- Later I put my calculations into schematics and simulate. I had to adjust my transistor sizes to increase gain and put $V_{outDC} \approx 1.5 V$ for better voltage swing.

Conclusion (Before layout):

With two stage op-amp we were able to obtain very high gain (~80dB) with bandwidth of ~1kHz. To be able to obtain this much gain, I had to use huge transistors (172 μ and 84 μ). On the other hand I was able to work with low power (~300 μ W) while satisfying Slew rate requirement (~5.6 V/ μ s). My amplifier provides good power supply rejection ratio for both V_{DD} and V_{SS} (ground) (both ~80dB), if I calculate them correctly. I was able to obtain ~2.5 V voltage swing with a little distortion at minimum value and ~3 V voltage swing with a little distortion at minimum value (signal is still in sine shape). I had to adjust results of my calculations a lot to get my design working, like previous labs. My initial values and adjusted Width values are different.



I was able to fit my design in 29.97 x 62.295 rectangle Note: I change the order of capacitor and resistor

DRC, LVS and QRC (First)







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After layout W_{tot} decreased to ~266 $\mu W\!,$ nearly half of maximum value V_{outDC} increased to ~1.8 V



Av decreased to ~79.73 dB, ~ 96939.3 V/V which is ~3% lower than required $f_{upper3dB}$ decreased to ~910.1Hz, thus GBW ≈ 8.82 MHz ~11.8% lower than required



 $PM = \sim 63.1$ degree as expected



Slew rate decreased to \sim 5.23 V/µs, still 4.6% higher than required.



I was able to obtain ~ 2.5 V output voltage swing



 $A_{dd}\approx$ -0.528 dB thus $PSRR_{Vdd}\approx$ 80.256 dB, more than double of required



 $A_{ss} \approx$ -10.01 dB thus $PSRR_{Vss} \approx 89.73$ dB, more than double of required

Conclusion (After First Layout):

With two stage op-amp we were able to obtain very high gain (~80dB) with bandwidth of ~900Hz. Size of resulting amplifier is roughly 30 x 62.3. It is huge due to large sized transistors (M1, M3, M4 in layout) and compensation capacitor. Width (62.3 one) can be made smaller by squeezing components between M4 and capacitor. On the other hand my op-amp draws even less current than schematic, resulting $P_{tot} \approx 266 \mu$ W, without violating slew rate requirement (SR $\approx 5.23 \text{ V/}\mu$ s). My op-amp provides even better power supply rejection ratio for both V_{dd} and V_{ss} , ~80dB and ~90dB respectively. Voltage swing (~2.5 V) won't chance between layout and schematic, even through V_{outDC} increased ~0.4V. Between layout and schematic all values are changed. But still only two specifications are not satisfied gain (3% lower) and GBW (~11% lower).

Final Layout



I was able to fit my design in to 21.05 x 56.265 rectangle, ~36.56% smaller than my initial layout.

DRC, LVS and QRC (Final)



Yigit Suoglu 17720 Schematic (Final)



 $I_{tot} \text{ is decreased a little resulting } P_{tot} \approx 265.6 \; \mu W$

 V_{outDC} increased even more, to ${\sim}1.84~\mathrm{V}$

Simulation Results (After First Layout)



Av decreased even more, to ~79.70 dB, ~ 9660.5 V/V which is ~3.4% lower than required $f_{upper3dB}$ decreased to ~904.9 Hz, thus GBW ≈ 8.74 MHz ~12.6% lower than required



 $PM \approx 63.1 \deg$



Slew rate \approx 5.28, increased a little compared to first layout



I was able to obtain $\sim 2.5 V$ output voltage swing



 $A_{dd} \approx$ -0.526 dB thus $PSRR_{Vdd} \approx$ 80.229 dB, more than double of required



 $A_{ss} \approx$ -10.78 dB thus $PSRR_{Vss} \approx$ 90.49 dB, more than double of required

Conclusion (Final):

I was able to reduce area of my amplifier by 36%, however my gain and gain-bandwidth got worse. My gain is still roughly 3% lower than required and my gain-bandwidth is roughly 13% lower than required, which is too low. I was able to decrease power consumption and increase slew rate at the same time. My PSRR values changed opposite direction, for V_{ss} (ground) increased for V_{dd} decreased. I was able to obtain similar output voltage swing as my first layout.