# MMIC to Waveguide Interfaces for 20 GHz Applications


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***Abstract*—In this paper, contactless monolithic microwave integrated circuit (MMIC) to waveguide for W band is scaled up to work between 18 - 22 GHz. Contactless transition couples the electromagnetic fields between a Substrate Integrated Waveguide (SIW) and a ridge waveguide. This paper presents the design and the simulation results of the scaled version. Simulated insertion loss is less than 0.1 dB at 20 GHz for back to back configuration with approximately 34% fractional bandwidth.**



***Index Terms*—Microstrip line to Waveguide, Monolithic Microwave Integrated Circuit, Waveguide, Transition, Interconnect**


## I. Introduction

Waveguide and microstrip line are two frequently used transmission lines in high frequency circuit design. Microstrip lines are widely used to connect active and passive elements, such as monolithic microwave integrated circuits (MMICs). Waveguides are used to connect antenna and receiver/transmitter. Waveguides provide a very low insertion loss and a high quality factor, which makes them more appealing than microstrip lines. However, most MMICs does not have a waveguide output. Thus, an interface is required.

Waveguide to microstrip interfaces have been heavily researched. Most of them are designed to operate on W band, [1] – [5]. Reference [5] provides an interface with a waveguide transition chip made of an organic material. This second chip connected to a MMIC via wire bonding. This solution is able to provide $S_{11}$ below -10 dB and $S_{21}$ around -3 dB between 60 - 86 GHz in back to back transitions. Using a folded dipole antenna integrated in an embedded wafer level ball grid array, [3], provides a lower bandwidth and a lower insertion loss, 5 GHz and 2 dB respectively. A ridge structure on a high permittivity thin film material, [2], is a wideband and low insertion loss solution. Another wideband and low insertion loss design is proposed in [4] as an inline microstrip to waveguide transition. According to the simulation results, this design covers a larger frequency range than W band and has less than 0.55 dB of insertion loss. Even though previously mentioned designs are appropriate to scale to 20 GHz, [1] is selected to scale. The solution in [1] provides low insertion loss and high bandwidth in simulations.

Solutions for lower frequency bands are also available. An inline transition in the band 8.5 - 9.5 GHz is provided in [7]. This design provides maximum insertion loss of 1.5 dB in the band 8.5 - 9.5 GHz with a simple modular assembly. The wideband waveguide to microstrip interface at 15 - 27 GHz band with insertion loss lower than 0.13 dB is reported in [6].

## II. Stepwise Scaling and Simulations

In this section, a scaled versions of [1] with their simulation results are presented. Most of the provided dimensions are scaled from 92.5 GHz to 20 GHz. In this paper WR42 is used. WR42 is commonly used for applications in K band. Inner dimensions for WR42 are 10.668 mm x 4.318 mm, and the wall thickness is set to 1.016 mm. Both the substrate integrated waveguide (SIW) and microstrip line are on same alumina substrate ($\varepsilon_r$ = 9.9), but its thickness increased to 0.38 mm. Copper is used as a conductor, and its thickness on PCB is set to 35 µm.

CST Studio Suite 2018 Student Edition is used for 3D modelling and simulation. A frequency domain solver is used. This paper follows the same partition scheme as [1]. Individual parts are simulated using tetrahedrons and the complete interface is simulated using hexahedrons.

### A. Rectangular to Ridge Waveguide Transition

A three-step Chebyshev transformer based on quarter wave impedance matches is used. 3D model is shown in Fig. 1. The obtained dimensions of the 20 GHz design are: $H_r$ = 0.156 mm, $L_r$ = 2.776 mm, $H_1$ = 0.273 mm, $L_1$ = 4.288 mm, $H_2$= 0.922 mm, $L_2$ = 4.233 mm, $H_3$ = 2.778 mm, $L_3$ = 4.502 mm, and the widths of all sections $W_r$ = 2.99 mm. The waveguide ports are used at both sides. Simulation results are provided in Fig. 2.

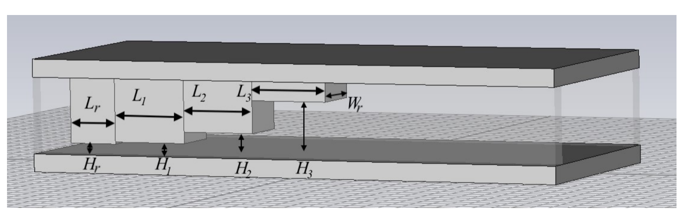


Fig. 1. 3D model of scaled rectangular to ridge waveguide transition. Waveguide side walls are transparent.

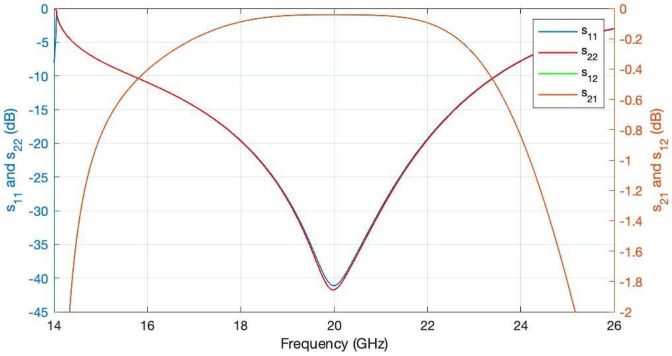


Fig. 2. Simulated S-parameters of scaled rectangular to ridge waveguide transition.

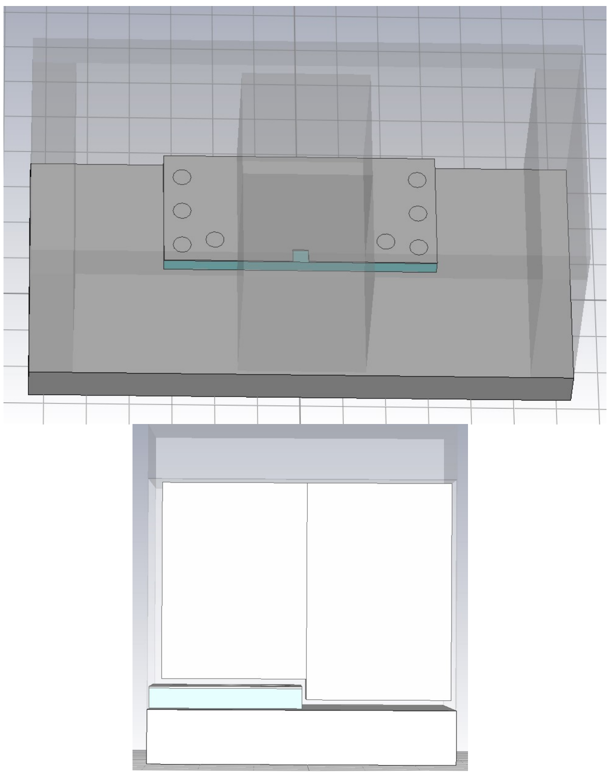

Fig. 3. 3D model of scaled ridge waveguide to SIW transition. Stub, ridge, waveguide side and top walls are transparent.

## B. Ridge Waveguide to SIW Transition

The ridge is extended with a stub with width of $W_{\mathrm{r}}$, same as the ridge, and the length $L_{\mathrm{stub}}$ = 2.776 mm. Distance between the top of the copper on the SIW and the lowest point of stub, $d_{\mathrm{stubSIW}}$ = 0.14 mm. In this part only SIW part of the dielectric is included. Width of the dielectric, $W_{\mathrm{d}}$ = 6.412 mm and length of the SIW, $L_{\mathrm{SIW}}$ = 2.907 mm. Radius of the vias, $r_{\mathrm{via}}$ = 0.2135 mm. Distance between centre of the first via and the sides of dielectric is $2r_{\mathrm{via}}$. Distance between the centre of the neighbouring vias are $d_{\mathrm{via}}$ = 0.94 mm. Two inductive tuning vias and a U-shaped notch are added similar to [1]. The distance between the centre of the tuning via and two closest perpendicular sides of dielectric are

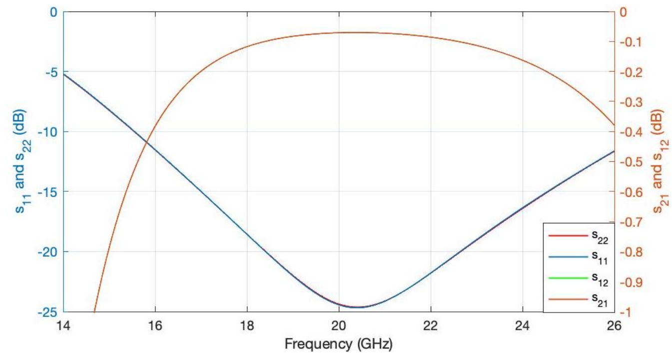


Fig. 4. Simulated S-parameters of scaled ridge waveguide to SIW transition.

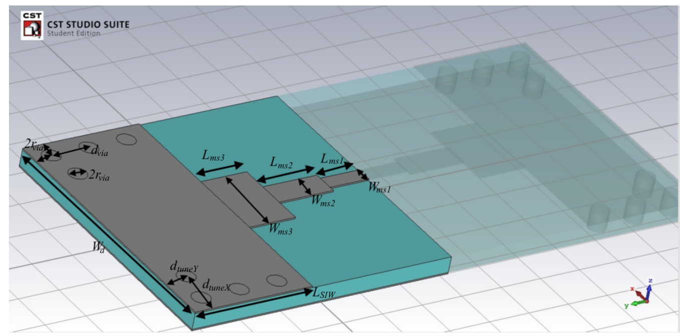


Fig. 5. 3D model of scaled SIW to microstrip line transition. Back to back configuration, second one is transparent.

$d_{\mathrm{tuneX}}$ = 1.197 mm and $d_{\mathrm{tuneY}}$ = 0.577 mm. The notch has dimensions of $W_{\mathrm{notch}}$ = 0.373 mm and $L_{\mathrm{notch}}$ = 0.319 mm. Distance between SIW and ridge is $d_{\mathrm{ridgeSIW}}$ = 0.088 mm. Fig. 3 presents 3D model. S-parameters are given in Fig. 4. $d_{\mathrm{stubSIW}}$ and $d_{\mathrm{ridgeSIW}}$ are optimised to obtain better matching between 18 - 22 GHz. The optimisation has resulted in lower bandwidth for this part.

## C. SIW to Microstrip Line Transition

SIW is matched to a 50 Ω microstrip line using step-tapered microstrip line sections. The width of 50 Ω microstrip line is calculated to be $W_{\mathrm{ms1}}$ = 0.339 mm for used PCB.

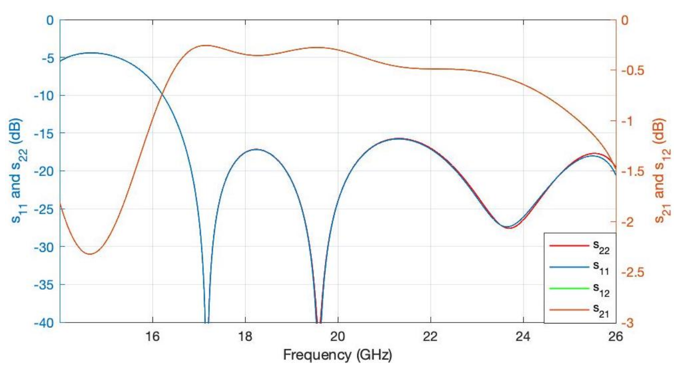


Fig. 6. Simulated S-parameters of scaled SIW to microstrip line transition for back to back configuration.

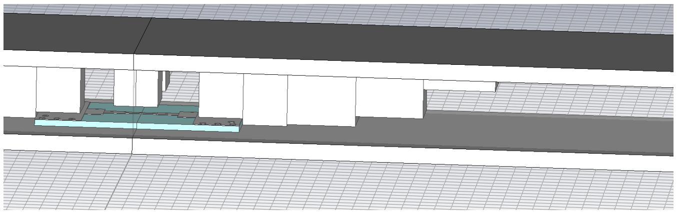

Fig. 7. 3D model of scaled final interface. Back to back configuration, side waveguide walls are transparent.

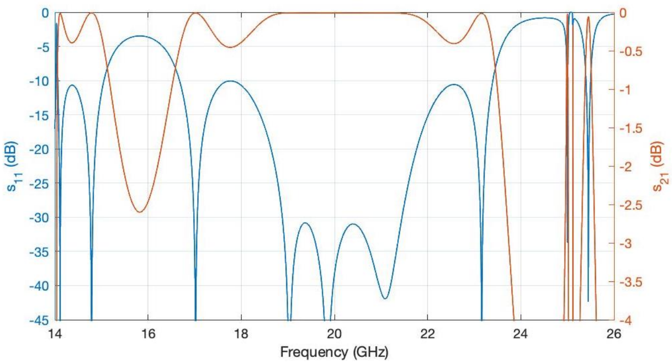


Fig. 8. Simulated S-parameters of final design, back to back configuration.

The length of the first section is $L_{\text{ms1}}$ = 0.983 mm. Dimensions of the other two sections follows as $W_{\text{ms2}}$ = 0.61 mm, $L_{\text{ms2}}$ = 1.368 mm, $W_{\text{ms3}}$ = 1.752 mm, and $L_{\text{ms3}}$ = 1.154 mm. SIW and via dimensions same as already presented. The notch is not included in this model. Fig. 5 was illustrates the 3D model in back to back configuration. Simulation of this module is also done in back to back configuration. Simulation results are provided in Fig. 6.

## III. Final Scaled Design

Combined length of all parts is 44.598 mm. Half of this length is WR42 waveguide and can be shortened if desired. The final design includes field blocking pins with the dimensions of $W_{\text{fbp}}$ = 3.02 mm, $L_{\text{fbp}}$ = 1.38 mm and $h_{\text{fbp}}$ = 1.2 mm. $h_{\text{fbp}}$ is the distance between lowest part of the field blocking pins and the top of the copper on the PCB. The distance between the centre of the model and the further part of the field blocking pins is $d_{\text{fbp}}$ = 4.26 mm. 3D model of the final interface in back to back configuration is provided in Fig. 7. The final design is simulated in 3 cases.

### A. Back to Back Transition

The first case is back to back transition. This is the same configuration as [1]. Microstrip ends connected to each other, the signal sent and received via waveguide ports. Simulation results provided in Fig. 8. Simulated return loss is better than 10 dB between 16.68 - 23.4 GHz (approx. 34% fractional bandwidth) and better than 20 dB between 18.67 - 21.74 GHz (approx. 15.6% fractional bandwidth). Simulated insertion loss is less than 0.1 dB at 20 GHz and better than 0.7 dB between 16.6 - 23.4 GHz. Compared to [1], simulation results of this design provides better insertion/return loses around the centre frequency and a lower fractional bandwidth.

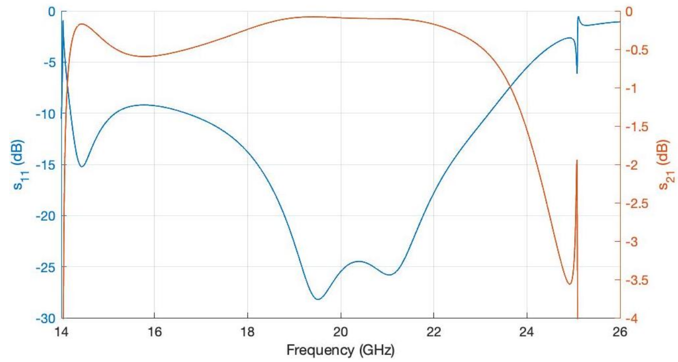


Fig. 9. Simulated S-parameters of final design, single transition.

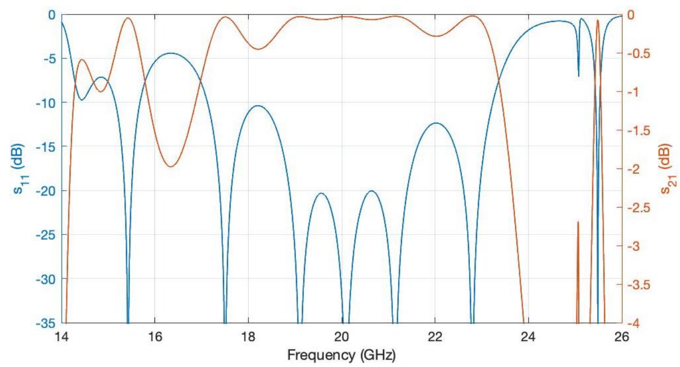


Fig. 10. Simulated S-parameters of final design, reverse back to back configuration.

### B. Single Transition

The second case is single transition. Waveguide end is connected to a waveguide port and microstrip end is connected to a discrete port with 50 Ω impedance. The simulation results are provided in Fig. 9. The simulated return loss is better than 10 dB between 16.68 - 23.19 GHz (approx. 32.6% fractional bandwidth) and better than 20 dB between 18.79 - 21.77 GHz (approx. 14.7% fractional bandwidth). The simulated insertion loss is less than 0.1 dB at 20 GHz and better than 0.5 dB between 16.7 - 23 GHz.

### C. Reverse Back to Back Transition

The last case is reverse back to back transition. Waveguide ends connected together and microstrip ends connected to discrete ports with 50 Ω impedance. Total waveguide length is reduced, because increased mesh count is greater than student licence allows. The simulation results are provided in Fig. 10. The simulated return loss is better than 10 dB between 17.12 - 23.24 GHz (approx. 30.3% fractional bandwidth) and better than 20 dB between 18.82 - 21.4 GHz (approx. 12.9% fractional bandwidth). The simulated insertion loss is less than 0.1 dB at 20 GHz and better than 0.5 dB between 17.12 - 23.23 GHz.

## IV. Conclusion

In this paper, contactless and bondwire-free MMIC to waveguide interface for W band is scaled, simulated and optimised for 20 GHz. Simulation results show low insertion loss and more than 20% fractional bandwidth for all simulation cases. Furthermore, the simulation results provide low in band ripples, especially for the back to back case. Scaled simulation results provided similar results as [1] without any optimisation. After optimisation, better insertion/return loses with lower bandwidth are obtained.

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