Design of RF Transistor Amplifier at 990 MHz

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***Abstract*—This paper presents design process of transistor amplifier designed to operate mainly at 990 MHz, but also between 841 MHz - 1.244 GHz without constant gain throughout whole band. Simulation results provide desired result. However due to the unknown error, measurement results does not provide similar results as simulation results.**

Keywords— RF amplifier

I. Introduction

Since the wavelength of the signal is comparable to the physical length of the system at higher frequencies many laws, such as Kirchhoff's laws, fails. Thus, amplifier designs at RF differ significantly from conventional low frequency designs. In addition to bias network and transistor, a RF transistor amplifier should have input and output matching networks.

This paper divided into six sections. First section presents design process on Agilent ADS. Than, at next section simulation results were presented. At section IV, production phase argued. Section V presents measurement results and argument about simulation and measurement results. Next section presents some mistakes of layout design, and how should to improve it. And finally a summary of this process provided.

II. Design

Both schematic and layout of amplifier was designed using Agilent ADS. This amplifier is designed on a FR-4 with ε_r of 4.6, dielectric thickness of 1.6 mm and conductor thickness of 35µm. As an amplifier Infineon BFP420 is used.

A. Schematic Design

As a first step of schematic design, a RF choke was designed to provide DC bias to the amplifier. As RF choke a shorted transmission line with λ/4 length is used. Three capacitors were placed between ground and transmission line as a DC block for bias voltages. RF choke is presented at fig 1.

Next step was to determine bias voltages and obtain s-parameters of determined bias voltages from s2p files of amplifier. Initially selections were follows as (1).

$$V_{CE} = 3.5\ V \text{ and } I_C = 35\ mA. \quad (1)$$

After selecting bias conditions and obtaining s-parameters for bias selected conditions, with the help of smith chart tool output and input matching networks were designed.

Later designed input and output matching networks connected to the transistor and DC blocking capacitors added. DC blocking capacitors were used as part of matching network. Using tuner matching networks were adjusted to provide better

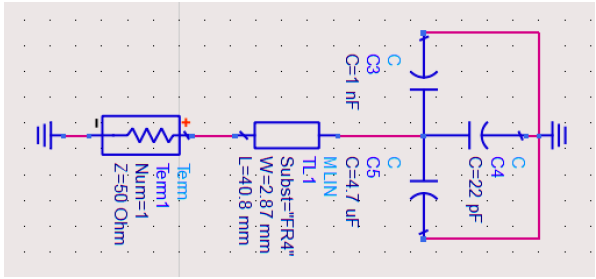

Fig. 1. RF choke

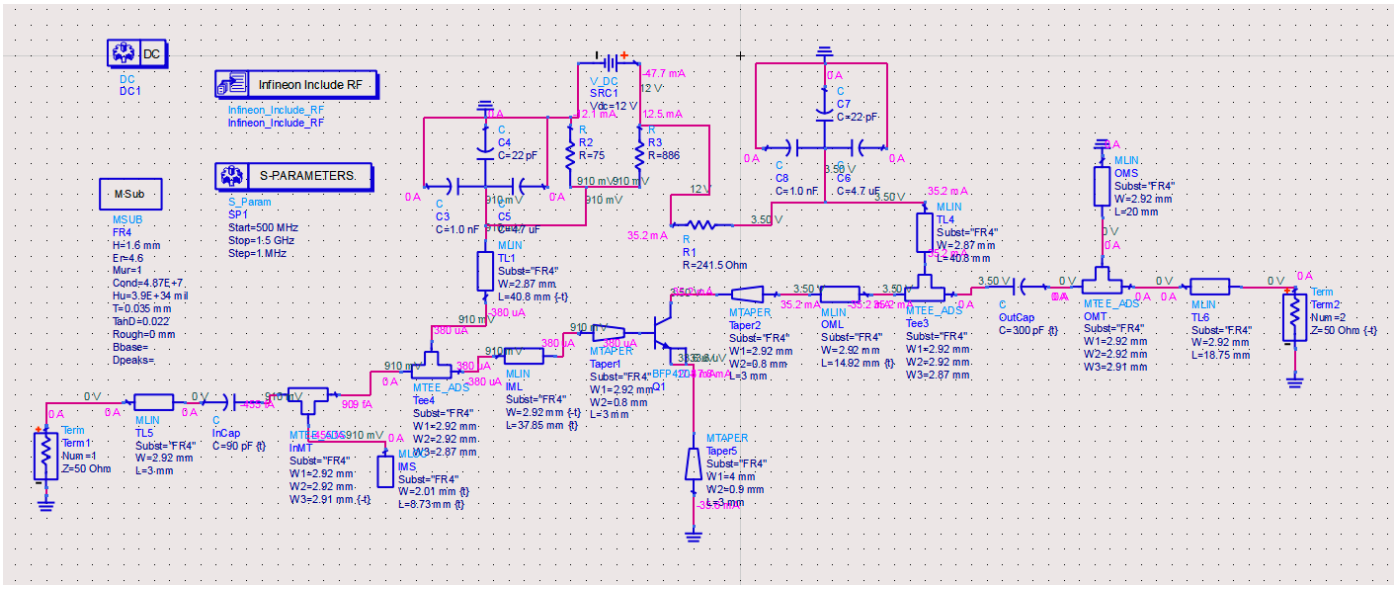

Fig. 2. Schematic design of RF transistor amplifier at 990 MHz

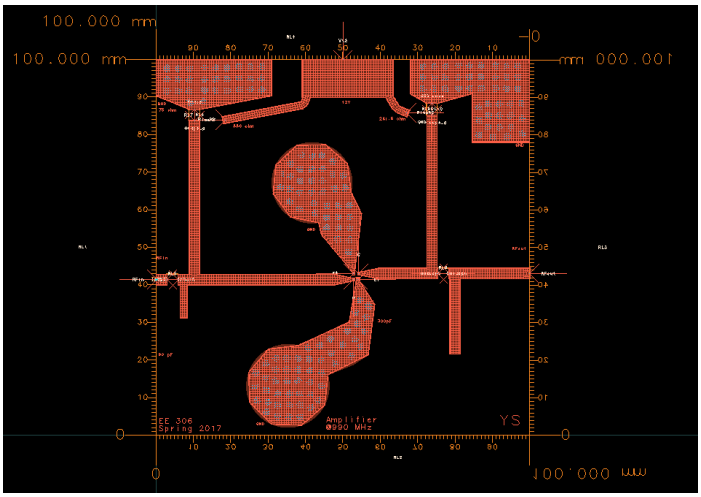

Fig. 3. Layout design of RF transistor amplifier at 990 MHz

s-parameters. s_{11} and s_{22} were set such that they provide less than -10 dB at 100 MHz above and below of 990 MHz incase of a frequency shift during manufacturing. Schematic design is provided at fig. 2.

B. Layout Design

First step of layout design was drawing footprint of transistor. Later, all transmission lines automatically generated by ADS; connected with each other and transistor footprint. That step followed by drawing of DC plate and ground plates. Its observed that without vias at ground planes extracted model has many parasitic elements which should not exist. Thus, simulation results differ a lot from schematic simulation. This problem solved by adding vias to ground plates at above. Fig 3 illustrates layout design.

III. Simulation Results

A. Schematic Design

Fig. 4 provides simulation results for schematic design. Schematic simulation results provide good s_{11} and s_{22} parameters at 990 MHz, -24.8 dB and -20.6 dB respectively.

B. Layout Design

Fig. 5 provides s-parameter simulation results for EM simulated transmission lines. For EM simulation momMW mod is used. Layout simulated using bias conditions at (2). Bias values at (2) obtained during production and verified with layout simulation.

$$V_{CE} = 3.35 \text{ V and } I_C = 25 \text{ mA}. \quad (2)$$

Designed amplifier does not provide its best results at 990 MHz. However, it provides good s_{11} and s_{22} parameters, -13.5 dB and -17.5 dB respectively.

Best working frequency of this amplifier is near 935 MHz, where it provides the best s_{11} and s_{22} parameters, -15 dB and -42.7 dB respectively. Also s_{21} parameter is just above 20 dB.

This amplifier provides acceptable s_{11} and s_{22} parameters, less than -10 dB, between 841 MHz to 1.244 GHz. However, s_{21} parameter is not constant throughout whole band. It is around 20 dB at lower frequencies and drops down to 16 dB around 1.2 GHz.

s_{12} parameter is below -20 dB for all simulated frequencies.

Fig. 6 provides power gain, stability factor and stability measure. Power gain has similar values to s_{21} parameter. The stability factor is greater than unity and the stability measure is

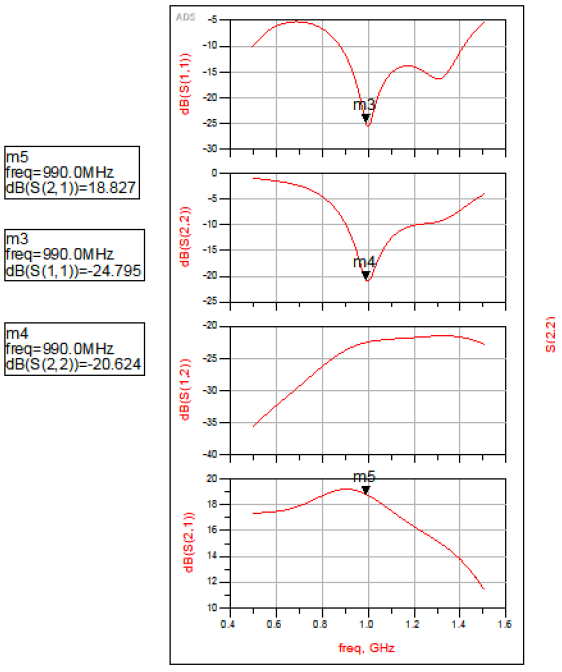

Fig. 4. Schematic simulation results

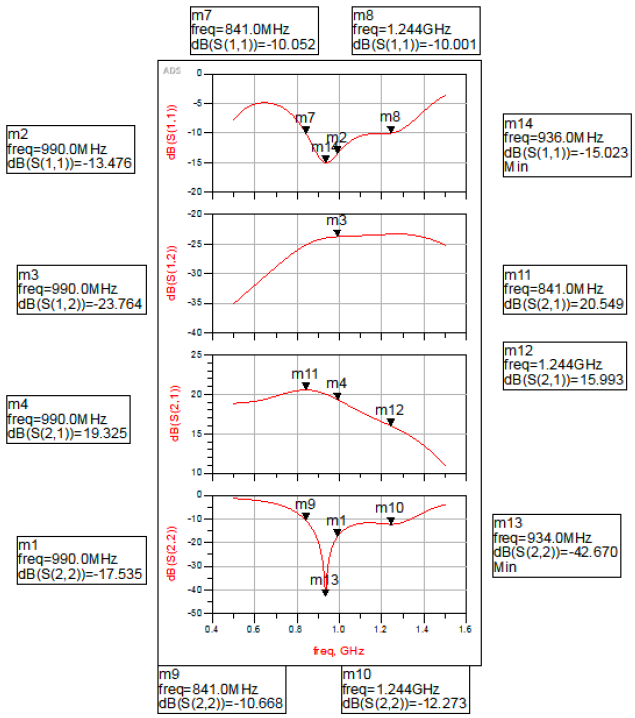

Fig. 5. Layout simulation results

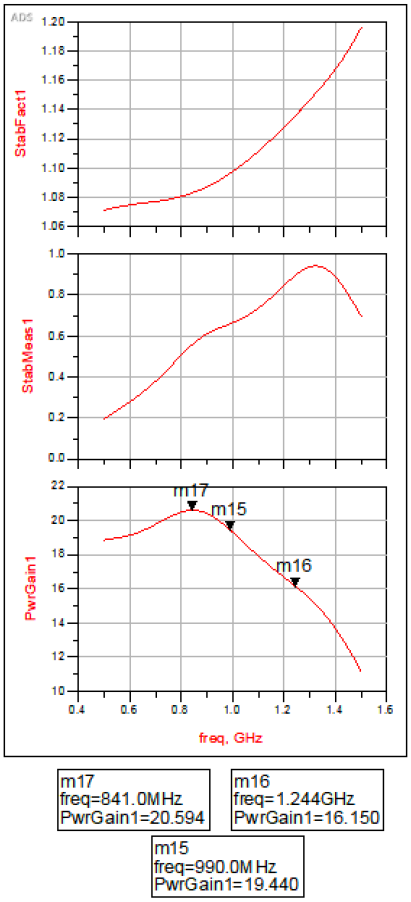

Fig. 6. Layout simulation results for stability and power gain

positive for whole band. Thus, designed amplifier is unconditionally stable for whole band.

IV. Production

A. PCB

Production step starts with printing the mask of designed amplifier. Two printed copies painted to a darker black with a permanent marker. Than those two copies of mask put on top of each other and prepared PCB. Preparation of PCB starts with cleaning copper plates. Then in a dark environment photoresist is applied to top of the PCB and put into oven to dry. After mask put on PCB, UV light was applied for 240 s. After UV light applied, PCB bathed in NaOH and H_2O to dissolve photoresist that is exposed to UV light. Later, PCB is washed with water and lights turn on. Ground plate is covered with tape to protect it from acid. As a final step PCB was bathed with mixture of H_2O_2, HCl and H_2O. And washed with water and nail polish remover. This concludes PCB production.

B. Components and Bias Network

First vias drilled on ground plates at top plate. Than this vias connected by putting wire and soldering it to top and bottom plates. Chip capacitors and SMA connectors were soldered to corresponding parts of transmission line. Later bias resistors were soldered. And finally transistor was soldered to its footprint. Biasing transistor was the hardest part. Initially 12 V DC voltage applied to bias network. However, many transistors were burned during testing bias networks. And many resistor combinations tried. During changing transistors collector footprint and taper connected to that footprint damaged. To fix damaged transmission, a copper wire was soldered between collector pin of transistor and transmission line. During biasing applied DC voltage decreed to 5 V from initial 12 V. β value of simulated transistor and actual β value of transistor varies significantly. Thus, simulated DC values and actual DC values does not correlate. After bias network formed three capacitors with different order of capacitances were soldered between V_{CC} and GND. Fig. 7 shows produced transistor amplifier.

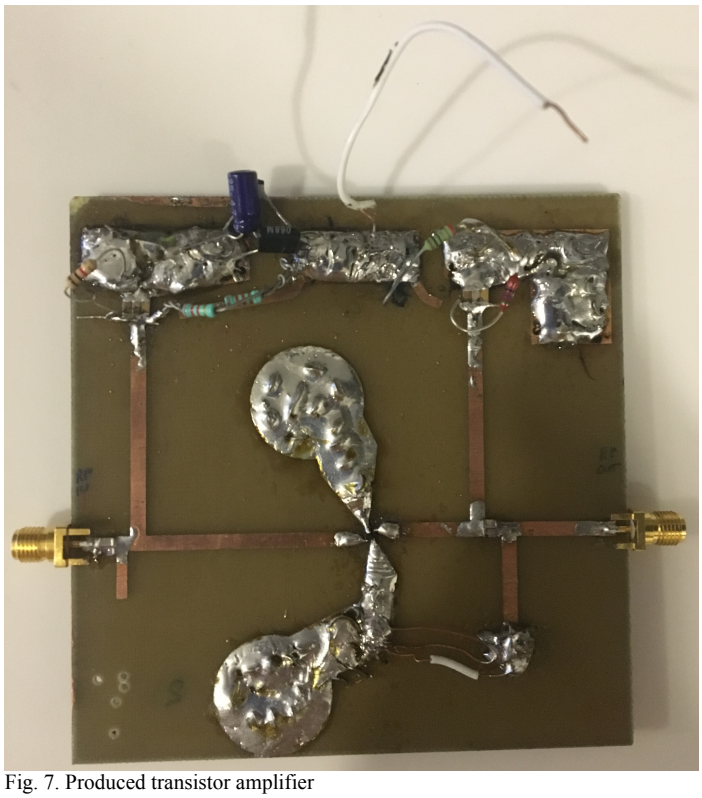

Fig. 7. Produced transistor amplifier

V. Measurement

Fig 8. provides measurement results. s_{22}, s_{12} and s_{21} parameters shows similar patterns as simulated results. Magnitude of s_{21} is much lower than simulated results and magnitudes of s_{22} and s_{12} are higher than simulated results. I believe this is because of the unknown error that affects s_{11} parameter. s_{11} is much higher than simulated results, it is nearly flat. Fig 9 provides detailed representation of s-parameters.

Measurement results for 990 MHz follows as:

- s_{11} = -5.16 dB
- s_{12} = -18.55 dB
- s_{21} = 11.99 dB
- s_{22} = -27.97 dB

s_{11} results are higher than -10 dB for all frequencies.

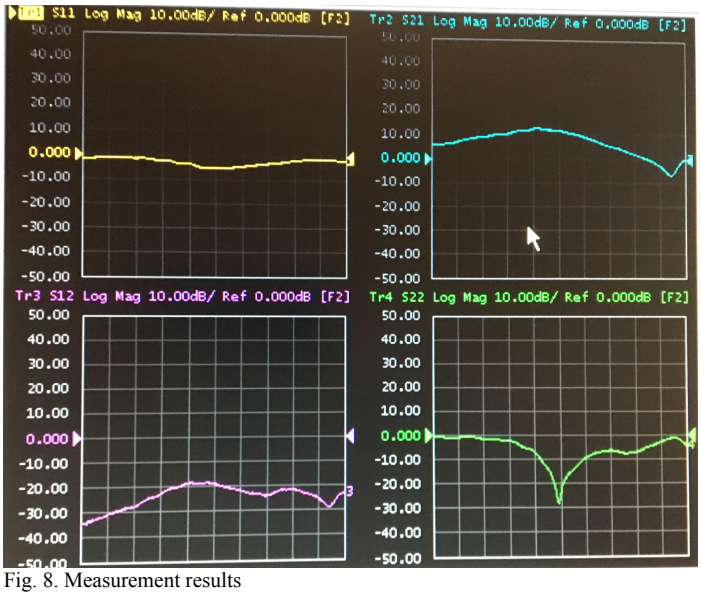

Fig. 8. Measurement results

VI. Required Improvements

Layout design needs many improvements. RF chokes should be thinner to increase Z_0 of line. Thus, making them better open circuit. Also size of the ground plates at the top side of PCB should be increased a lot. At least from the edge of the PCB to ground connection of short sub should be covered with ground plate.

VII. Conclusion

In this project, a transistor amplifier with operating frequency 990 MHz is designed. EM simulation results show unconditionally stable amplifier with acceptable, below -10 dB, s-parameters between 841 MHz and 1.244 GHz and without constant gain. On the other hand, measurement results show very high s_{11} parameter. Possibly effecting other s-parameters badly. Cause of this difference between measurement and simulation results is unknown but I suspect it might be the damage at collector end of transmission line.

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References

1. ADS Help

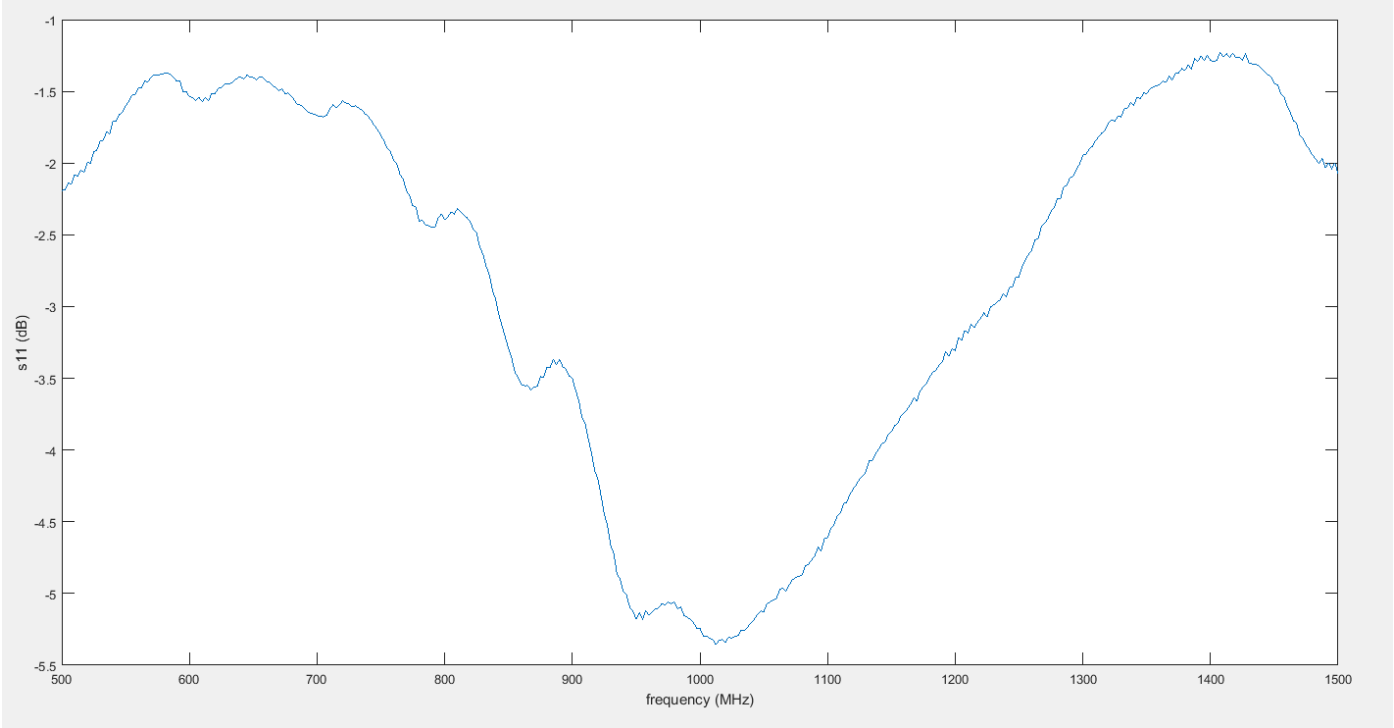

Fig. 9. Detailed measurement results

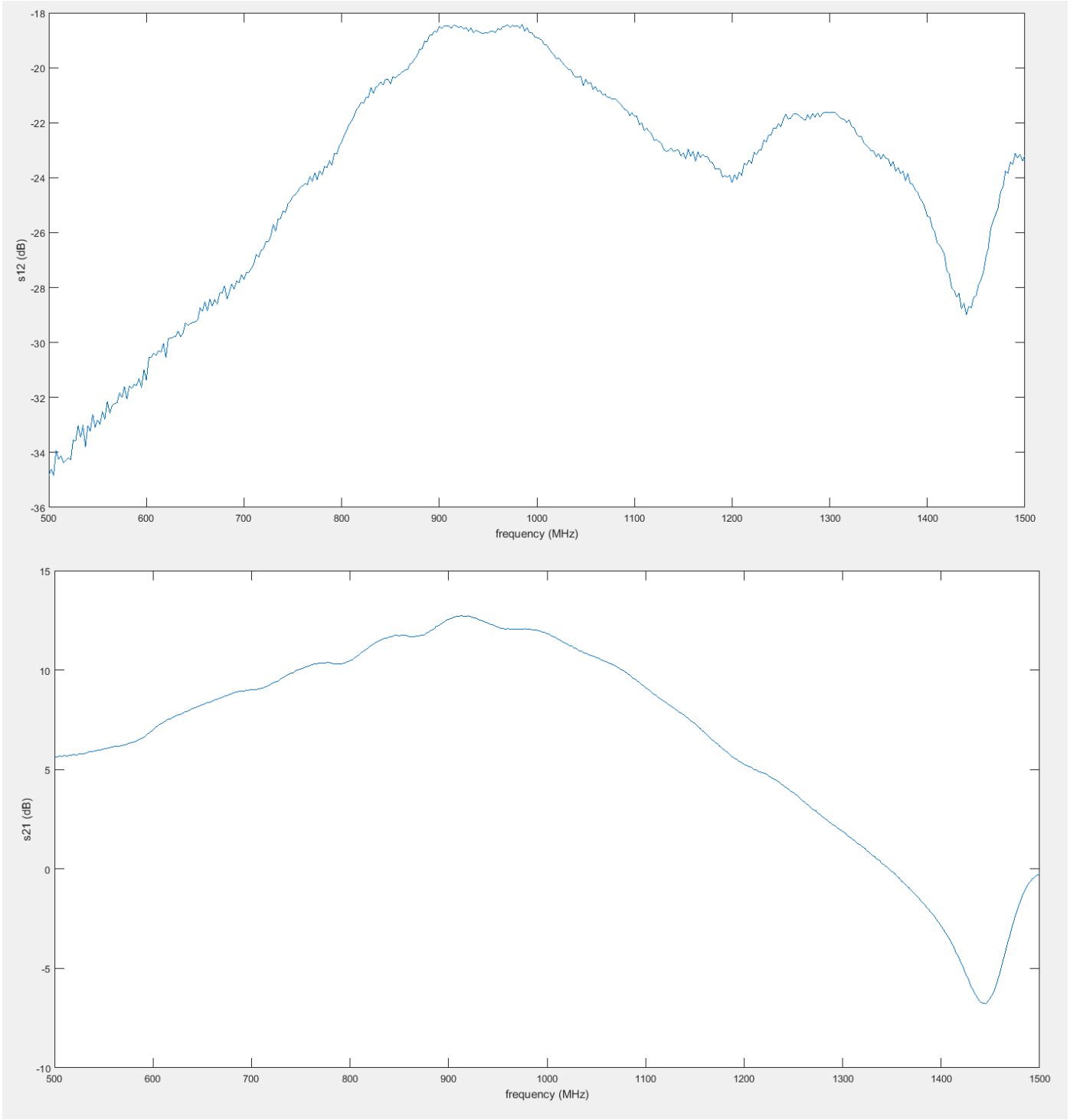

Fig. 9. Detailed measurement results (cont.)

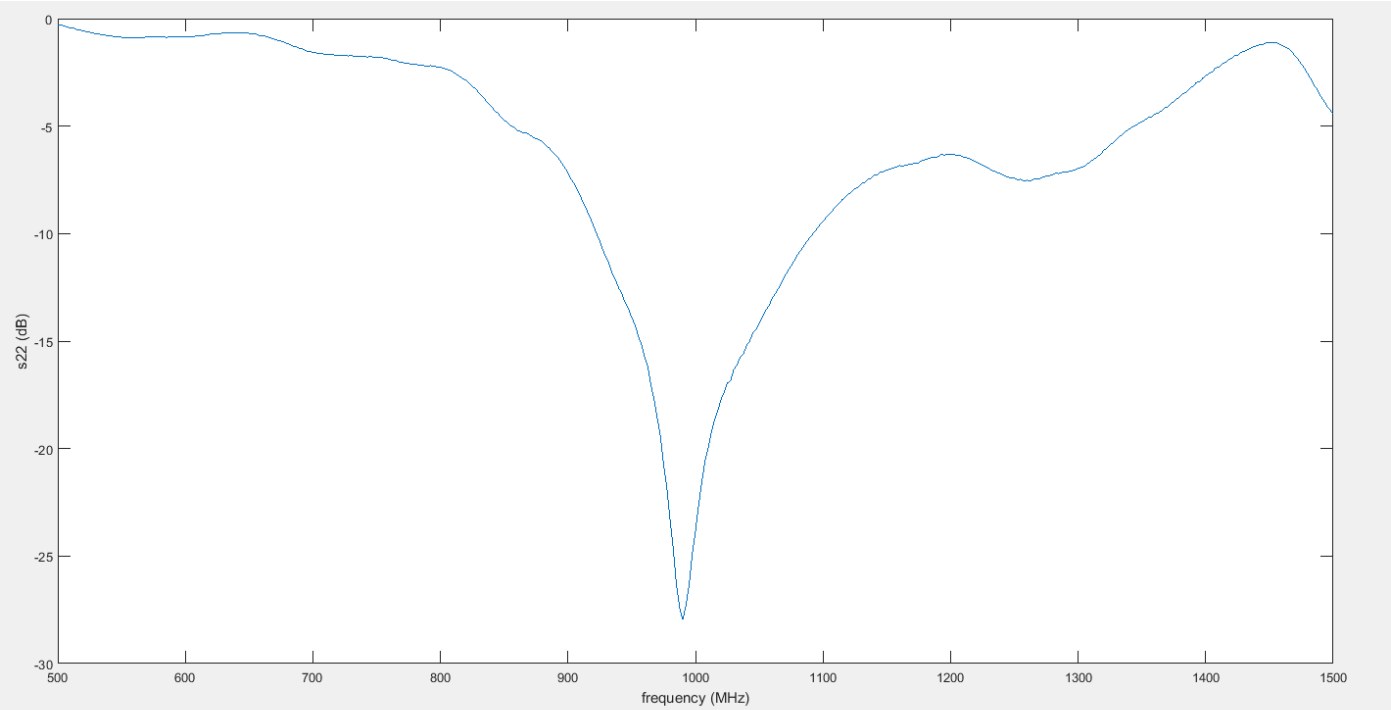

Fig. 9. Detailed measurement results (cont.)