Schematic Design of Full Differential Folded Cascode Operational Transconductance Amplifier

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Contents

1 Introduction

This report presents a schematic design of full differential folded cascode operational transconductance amplifier (OTA). Designed amplifier provides stable open loop gain and phase margin between -40 C° and 125 C°. Moreover power consumption of OTA is 175.9μW at 25 C° and OTA designed with X-FAB 0.18μ technology, XH018. And, the supply voltage of 1.8 V.

During this report, design of sub circuits that are used in full differential folded cascode OTA is also presented. Those are:

- Symmetrical OTA
- Bandgap reference circuit
- Gain boosting OTAs

2 Simulation Setup

During this section simulation setups for designs were argued. First subsection presents settings for simulations. And, second subsection presents test circuits used for simulations.

2.1 Simulation Settings

HSPICE was used for simulations. Simulation settings divided into four. First subsection provides simulation settings for normal simulations and temperature sweeps. Second subsection presents corner setups. And, third section provides Monte Carlo simulation. Last section shows outputs of these simulations.

Monte carlo simulation was only used on bandgap reference circuit. Corner simulations were used on all circuits except gain boosting amplifiers. Temperature sweep was used on both bandgap reference circuit and full differential folded cascode OTA. And, normal simulation is used at all circuits.

2.1.1 Normal Simulation and Temperature Sweep

At normal simulations temperature is set to 25 C°. And, temperature are swept between -40 C° and 125 C° with 2.5 C° intervals. For transient analysis highest accuracy and gear are selected, rest of the options are left as default values.

2.1.2 Corner Simulation

For corner simulations, 45 corners were selected. These corners were combinations of following parameters:

- V_{AVDD}: 1.62 V, 1.8 V, 1.98 V
- Temperature: -40 C°, 25 C°, 85 C°
- Transistor models:
  - w_p: fast NMOS & PMOS
  - w_s: slow NMOS & PMOS
  - w_o: fast NMOS & slow PMOS
  - w_z: slow NMOS & fast PMOS
  - tm: Typical

2.1.3 Monte Carlo Simulation

For monte carlo simulation 1000 samples have been selected and both __LOT__and __DEV__ parameters were set. All other settings set as default.

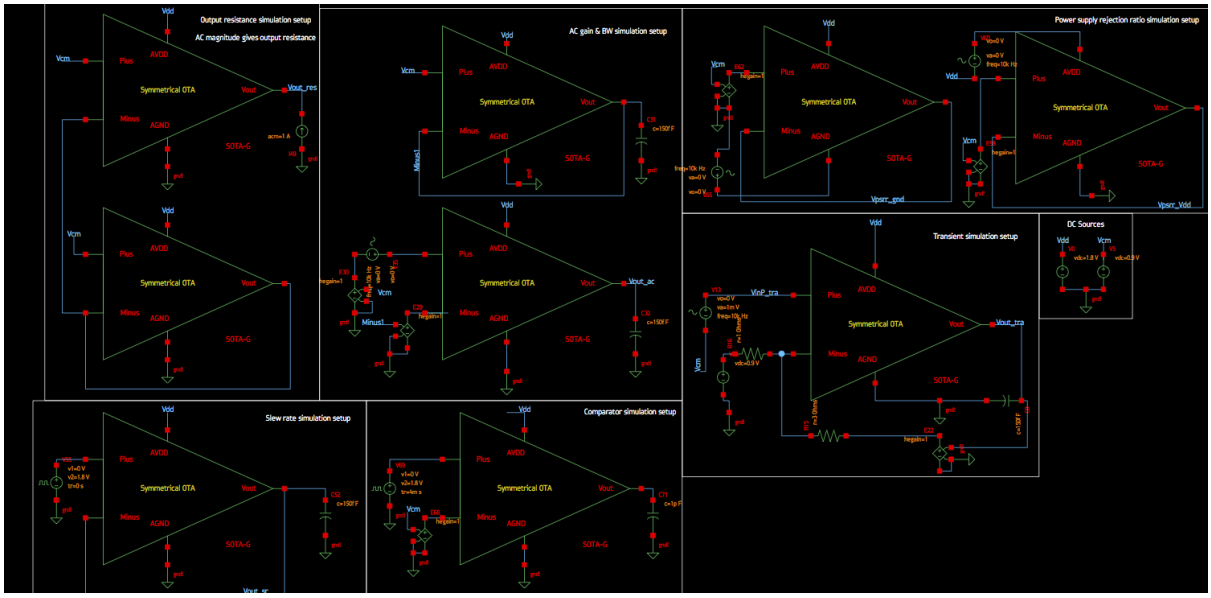

Figure 1: Test circuit for single ended OTA

2.1.4 Outputs

Simulation setups simulates for following parameters for OTAs:

- Open loop gain
- Phase margin
- Unity gain bandwidth (UGBW)
- 3 dB bandwidth
- Power supply rejection ratio for ground and VDD
- Output resistance
- Slew rate
- Transient gain for op amp, gain is controlled by the resistance ratio of the resistors
- DC operating points & power consumption

For bandgap reference circuit DC operating points and power consumption, and variation on reference voltage as ppm/C° is checked.

2.2 Test circuits

Test circuits divided into three according to their usage. All of the components used in test circuits are ideal. Component under test is put in to a "package". With this packaging method, test circuits can be used for many different design easily by changing only one instance instead of many.

2.2.1 Single ended output OTAs

Figure 1 provides test circuit used for single ended OTAs. Function each subcircuit is written in the rectangle that contains subcircuit itself. In some subcircuits another instance of the same design is used to create common mode voltage.

2.2.2 Bandgap reference

Bandgap reference circuit uses rather simple test setup. Supply ports connected to ground and a voltage source. Output port connected to a 150 fF capacitor.

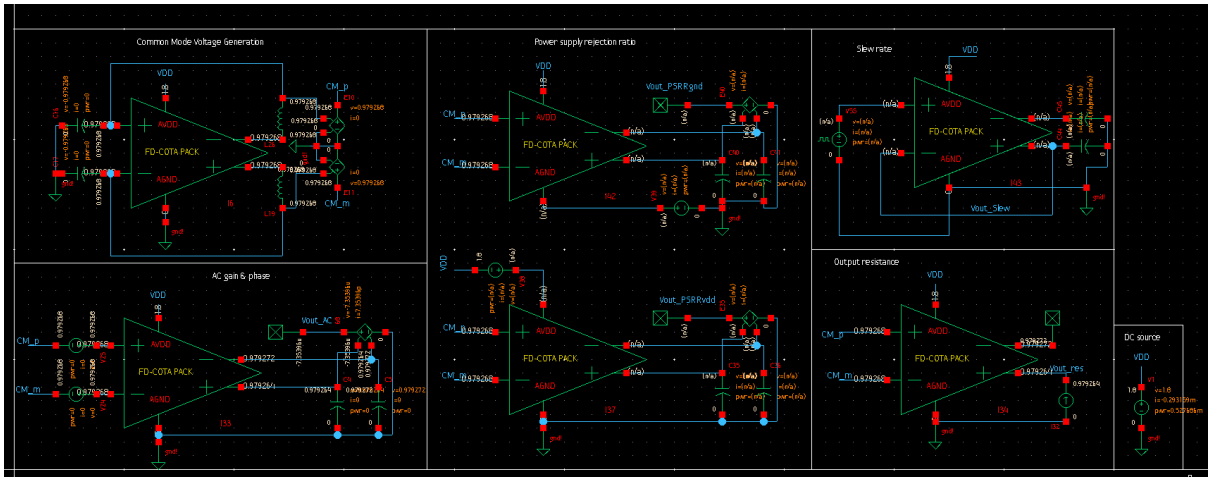

Figure 2: Test circuit for differential ended OTA

2.2.3 Differential ended output OTAs

Test circuit for differential ended output OTA is more organised than single ended one. (figure 1) Common mode voltage is generated in a subcircuit thats outputs were connected to voltage controlled voltage sources (VCVSs). Outputs of VCVSs were distributed other subcircuits. Figure 2 provides test circuit for differential ended output OTA. Similar to figure 1, function each subcircuit is written in the rectangle that contains subcircuit itself.

3 Symmetrical OTA

This section presents symmetrical OTA design, and divided into there subsections. First subsections provides device parameters and topology. Second subsections presents DC operating point and power consumption. And, last subsections presents remaining simulation results. Symmetrical OTA is used in the bandgap reference circuit.

3.1 Symmetrical OTA Design

Figure 3 provides schematic design of symmetrical OTA. Designed OTA employs NMOS differential inputs and generates bias voltage (Vbias) for the current source (M5).

3.2 Symmetrical OTA Operating Points

Figure 4 provides DC operating points of symmetrical OTA. From figure 4, $V_{outDC} = 0.900014$ V $\approx$ 0.9 V. And, $I_{Total} \approx 36.85$ μA. Thus, $P_{Total} \approx 66.33$ μW.

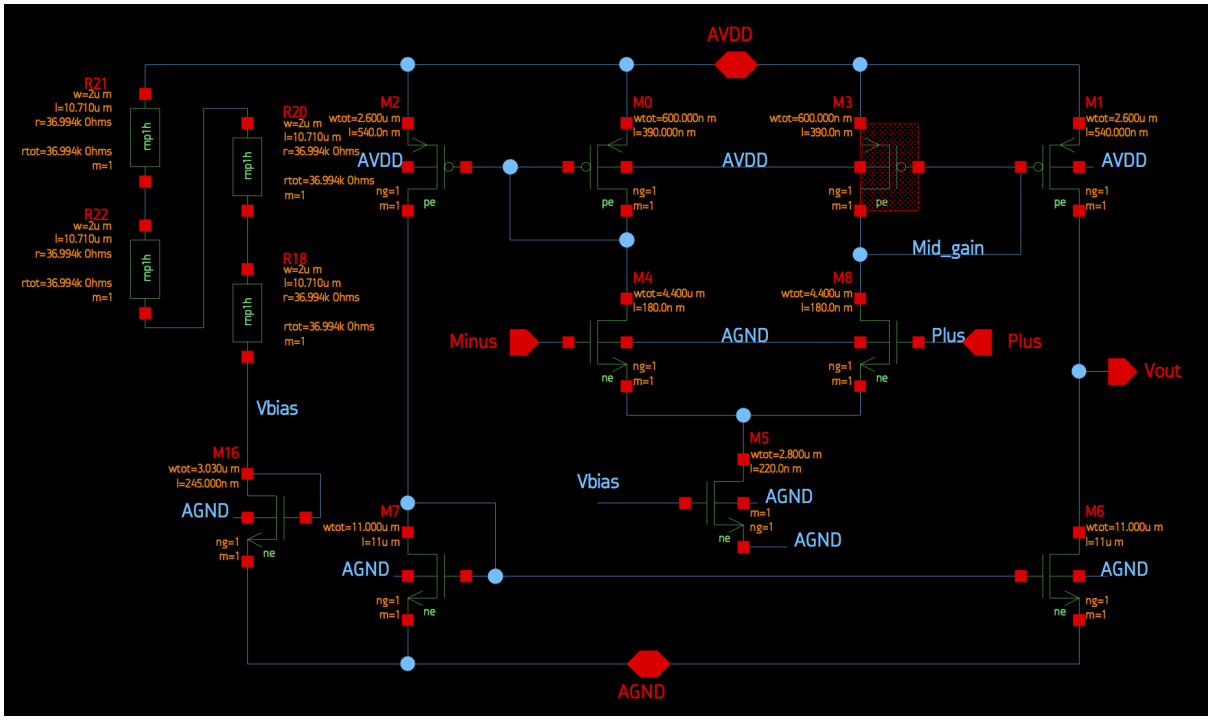

Figure 3: Device parameters of symmetrical OTA

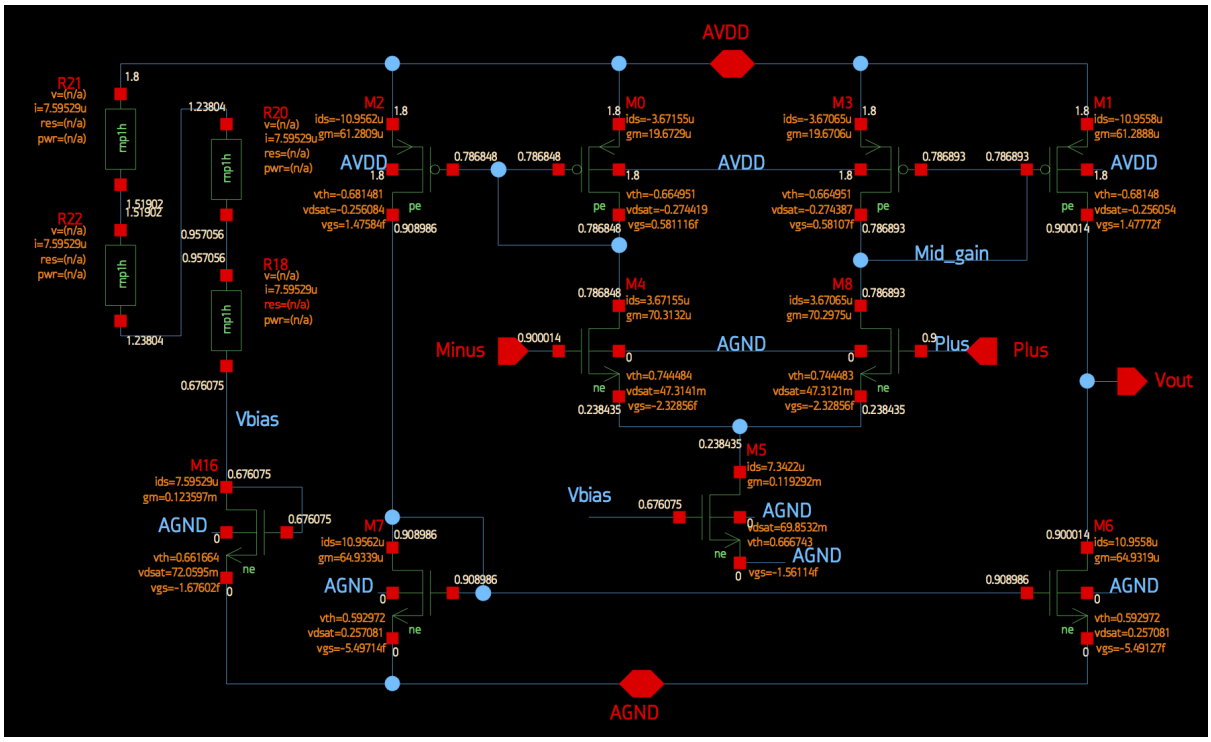

Figure 4: DC operating points of symmetrical OTA

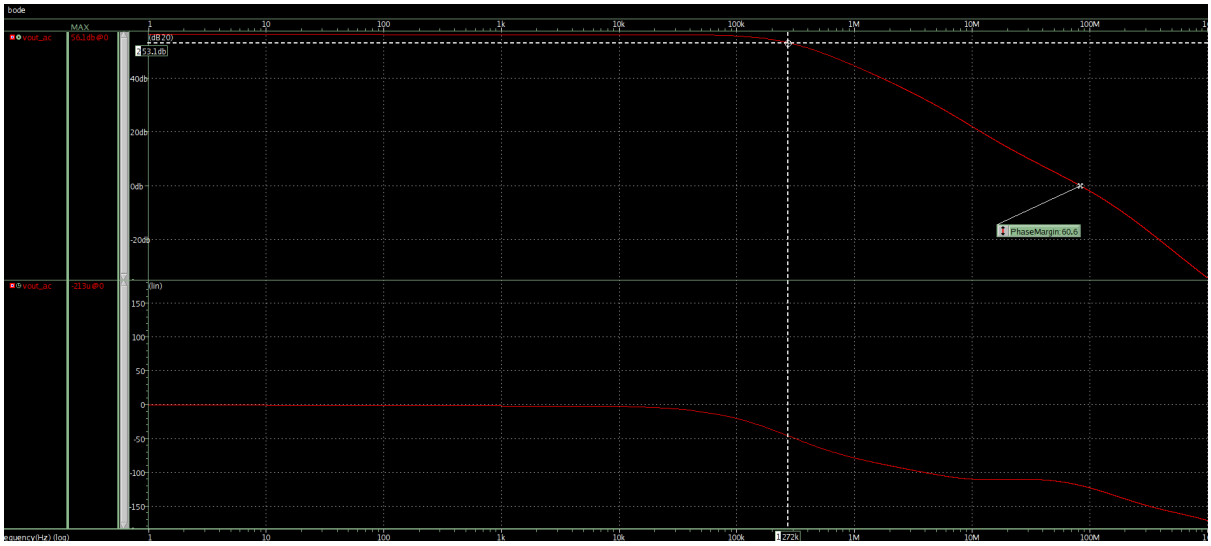

Figure 5: AC simulation results of symmetrical OTA

Table 1: Symmetrical OTA Simulation Results

Output	Value	Unit	Expression	Analysis
Open Loop Gain	56.1157	dB	db20(ymax(v(/Vout_ac)))	AC
PSRR GND	-58.1382	dB	db20(ymin(v(/Vpsrr_gnd)))	AC
PSRR VDD	-73.2357	dB	db20(ymin(v(/Vpsrr_Vdd)))	AC
Transient Gain	1.99397m	V/mV	peak2peak(v(/Vout_tra),n=0)	tran
Slew Rate	4.886679M	V/s	slewrate(v(/Vout_sr), 0.18,1.62,0)	tran
3dB Bandwidth	273.623k	Hz	bw3db(v(/Vout_ac))	AC
Output Resistance	3.25527M	Ω	(ymax(v(/Vout_res))	AC

Table 2: Symmetrical OTA Corner Simulation Results

Output	Unit	Minimum	Maximum	Mean	Standard Deviation
Open Loop Gain	dB	49.5265	59.7377	55.3553	2.73469
PSRR GND	dB	-61.2387	-52.1736	-57.4101	2.5279
PSRR VDD	dB	-108.681	-67.0945	-75.7501	6.85676
Transient Gain	V/mV	1.98766m	1.99601m	1.99320m	2.10228μ
Slew Rate	V/s	3.46634M	11.7832M	6.49062M	2.25575M
3dB Bandwidth	Hz	143.952k	682.725k	326.41k	158.216k
Output Resistance	Ω	1.30069M	6.1418M	3.42017M	1.55638M

3.3 Symmetrical OTA Simulation Results

Table 1 provides a table of simulation results for symmetrical OTA. And, figure 5 provides waveform of open loop gain simulation. From table 1 and figure 5; design provides 56 dB open loop gain, 60.6° phase margin, 90MHz of unity gain bandwidth (UGBW), 274kHz of 3dB bandwidth and 3.25MΩ of output resistance. These are approximate typical values.

Table 2 provides summary table of corner simulation results. Designed symmetrical OTA works on all corners. However specifications of amplifier varies from corner to corner a lot. This does not cause much problem since it is used in bandgap reference circuit.

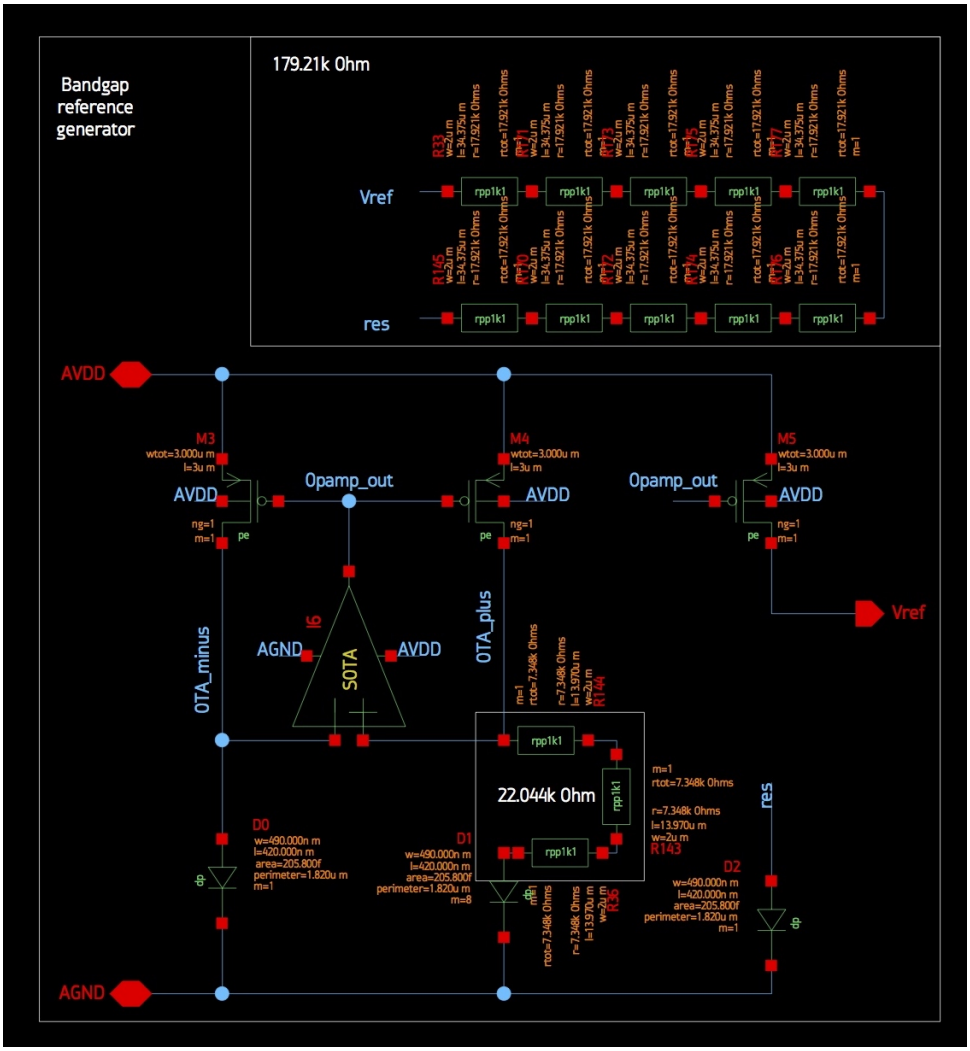

Figure 6: Bandgap reference circuit schematic design with device parameters

4 Bandgap Reference Circuit

This section presents the design and simulation results of bandgap reference circuit. Bandgap reference circuit is used to create a temperature independent voltage reference.

4.1 Bandgap Reference Circuit Design

Bandgap reference circuit employs a simple topology, provided at figure 6. The symmetrical OTA presented at the previous section used in design as instance I6. Opamp_out signal is a counter proportional to absolute temperature (CTAT) and is also used in the full differential folded cascode OTA to generate bias voltage. The design uses 2 rpp1k1 resistor groups, their values are written near them.

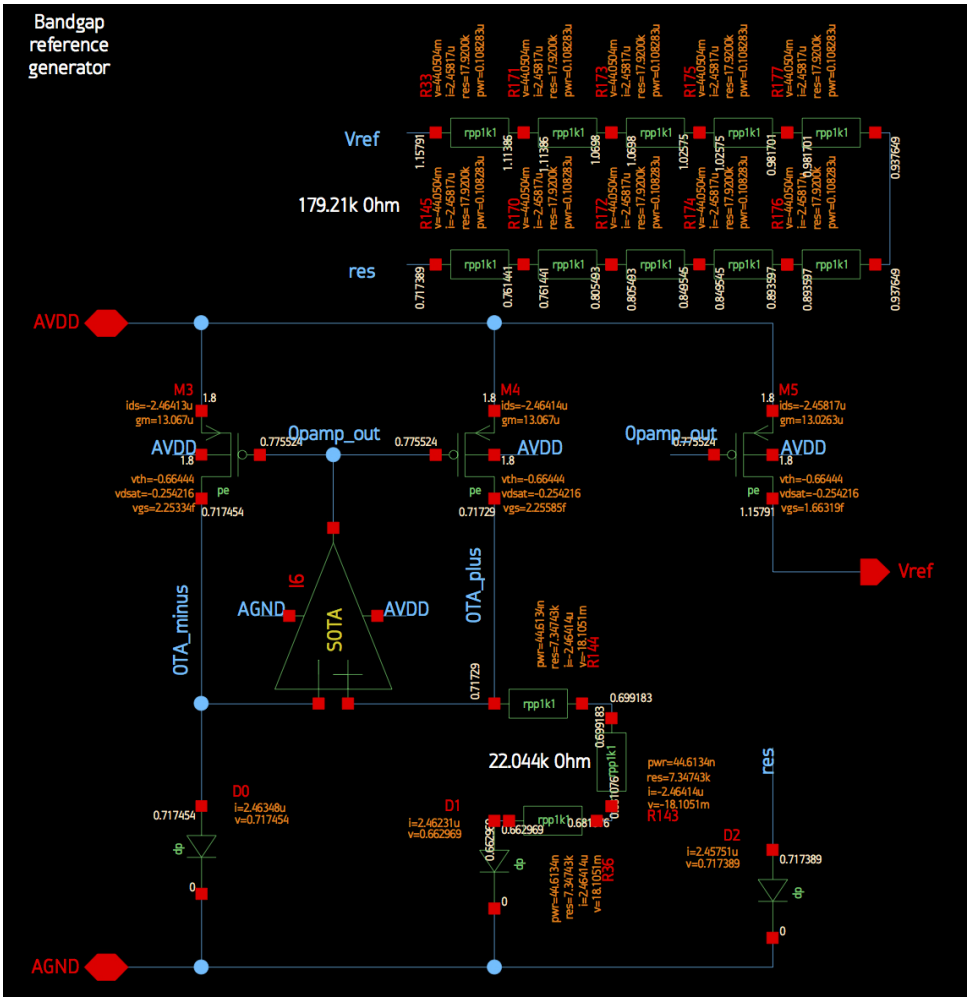

Figure 7: Bandgap reference circuit schematic design with operating points at 25 C°

Table 3: Bandgap Reference Circuit Simulation Results

Output	Value	Unit	Expression	Analysis
ppm	10.2415	10^{-6}V/C°	1.e6*(ymax(v(/Vref))-ymin(v(/Vref)))/165	DC

Table 4: Bandgap Reference Circuit Corner Simulation Results

Output	Unit	Minimum	Maximum	Mean	Standard Deviation
ppm	10^{-6}V/C°	10.0711	41.5787	19.7588	9.0182

4.2 Bandgap Reference Circuit DC Simulation Results

Power of the reference circuit simulated only at 25 C°. Using the results of figure 7 $I_{Total} \approx 7.38\ \mu A$. Thus, $P_{Total} \approx 13.29\ \mu W$. Power calculations does not contain the power dissipation of the OTA.

Designed bandgap reference circuit provides a reference near 1.75 V with 10.24 ppm variation. Figure 8 provides waveform view of reference voltage with respect to temperature. And, table 3 provides ppm (parts per million) result of the simulation.

Summary of the corner simulation results is provided at table 4. Even though worst corner results is around four times of the typical result, it is still quite low.

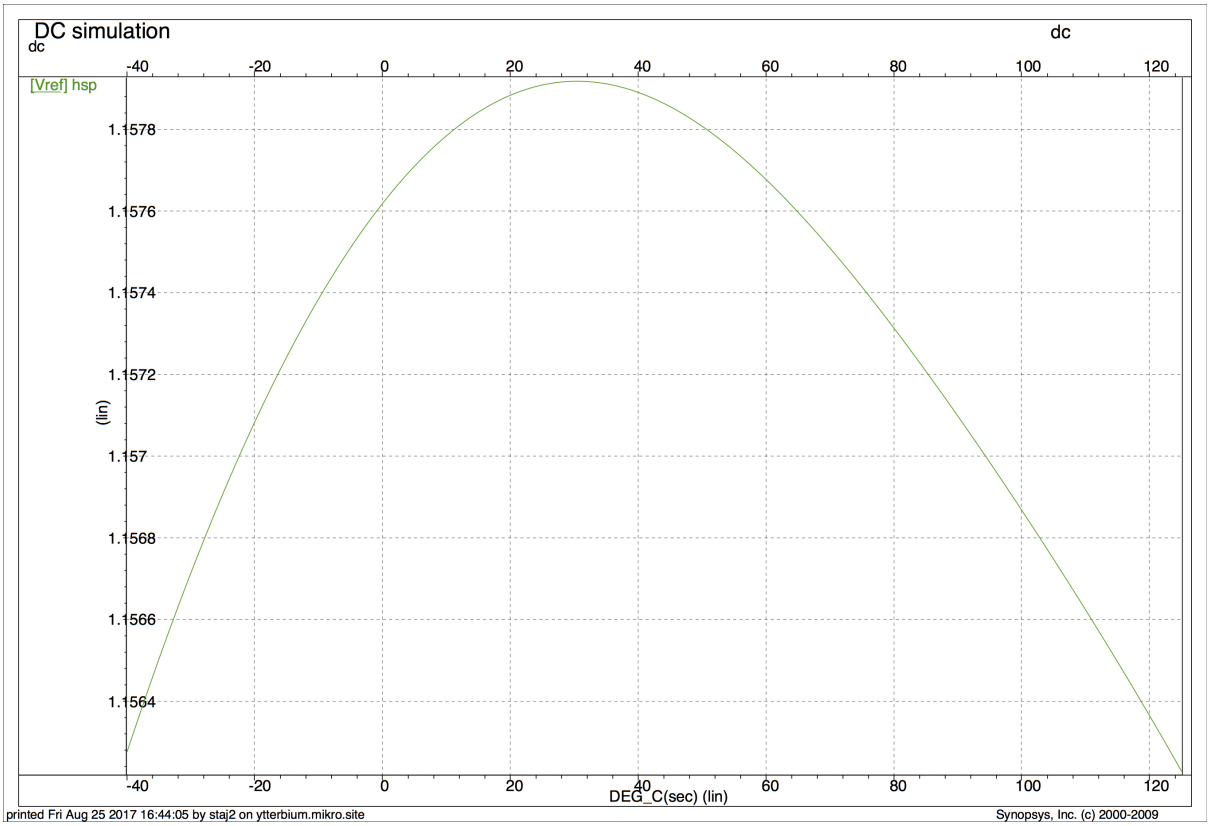

Figure 8: Bandgap reference circuit DC simulation results

On the other hand monte carlo simulation results were not good as corner results. Only 70.7% of the monte carlo simulation results achieve a ppm lower than 50. Statistical plot of monte carlo simulation results is provided at figure 9.

5 Fully Differential Folded Cascode OTA

This section presents the design of fully differential folded cascode OTA. Fully differential folded cascode OTA utilizes previously presented circuits to generate bias voltages. Moreover, it utilizes two more OTAs to increase its gain. These OTAs will be presented at next section.

Main objective of project was to achieve an open loop gain, phase margin and unity gain bandwidth independent of temperature (-40 C° to 125 C°) and supply voltage (1.62 V to 1.98 V). While temperature independence achieved to a some extent, final design is dependent of supply voltage. Final design achieves over 100dB open loop gain and around 70° phase margin.

5.1 Fully Differential Folded Cascode OTA Design

Fully differential folded cascode OTA has three subcircuits: amplifier, common mode feedback circuit and bias network; each presented in its own subsection.

5.1.1 Amplifier

Amplifier subcircuit is the subcircuit that amplifies small signal, thus the main part of circuit. Figure 10 provides schematic view of amplifier subcircuit. The design employs fully differential, PMOS input, folded cascode topology. It uses a common mode feedback circuit to keep the DC voltage of its outputs around 0.9 V. Common mode feedback circuit controls the bias voltage of current sources M5 and M6.

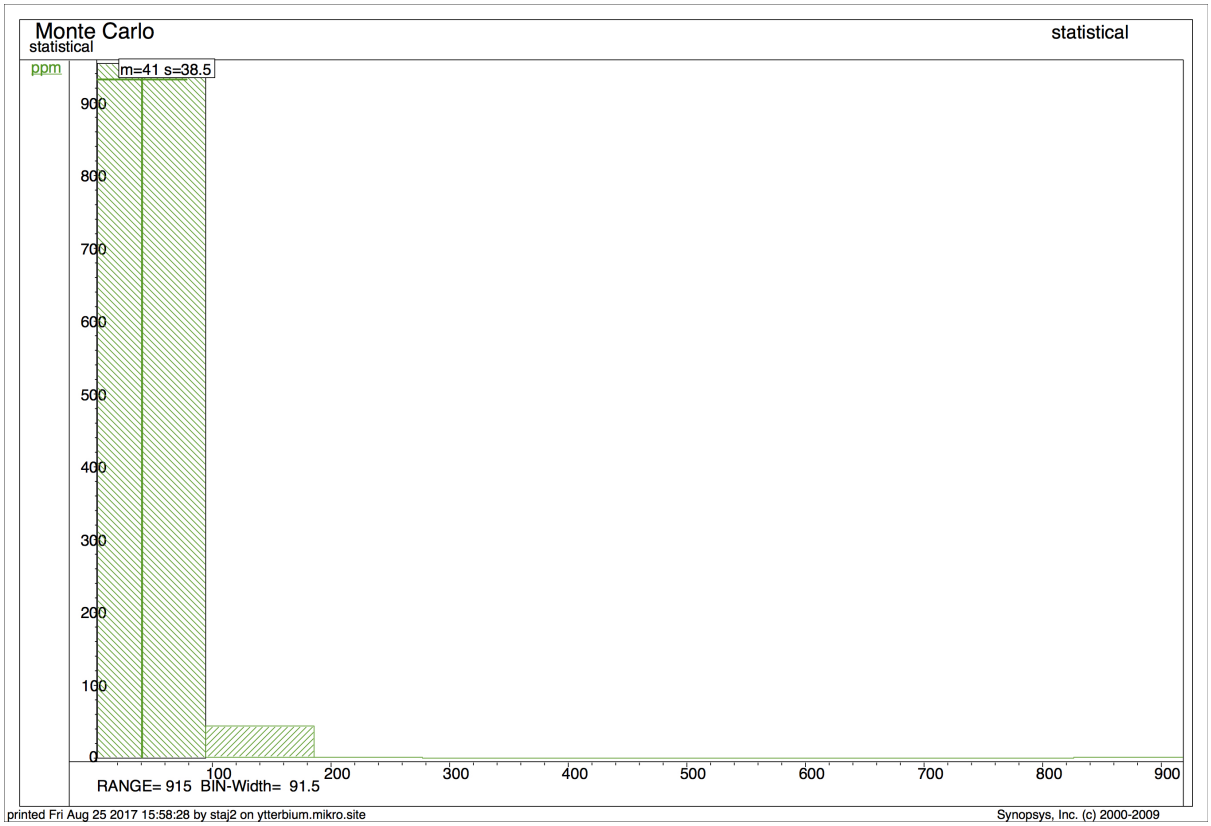

Figure 9: Bandgap reference circuit Monte Carlo simulation results

To increase the gain of amplifier, gain boosting amplifiers are used. NMOS input gain boosting amplifier controls the bias voltage of M3 and M4. PMOS input gain boosting amplifier controls the bias voltage of M7 and M8. Design of these gain boosting amplifiers will be presented at next section.

5.1.2 Common Mode Feedback Circuit

As previously discussed, common mode feedback circuit is used to keep the DC voltage of its outputs around 0.9 V by controlling the bias voltage of current sources M5 and M6. Schematic view of common mode feedback circuit is provided at figure 11.

Common mode feedback circuit is actually a part of bias network since it provides bias voltages for current sources M5 and M6. And, it takes its bias voltages from bias network.

Initially V_{CM} is set to 0.9 V. However, it is lowered to 0.86 V to decrease dependence to the temperature.

5.1.3 Bias Network

Bias network design to provide temperature independence to the amplifier. Bias network utilises bandgap reference circuit and common mode feedback circuit to create bias voltages.

Bias network mostly uses NMOS - PMOS transistor pairs. However, a diode and resistors were added to increase temperature independence.

Bias voltages generated by bias network are also used in bias network itself to create other bias voltages. With this method, it was possible to create a bias voltage with specific behaviour with respect to temperature.

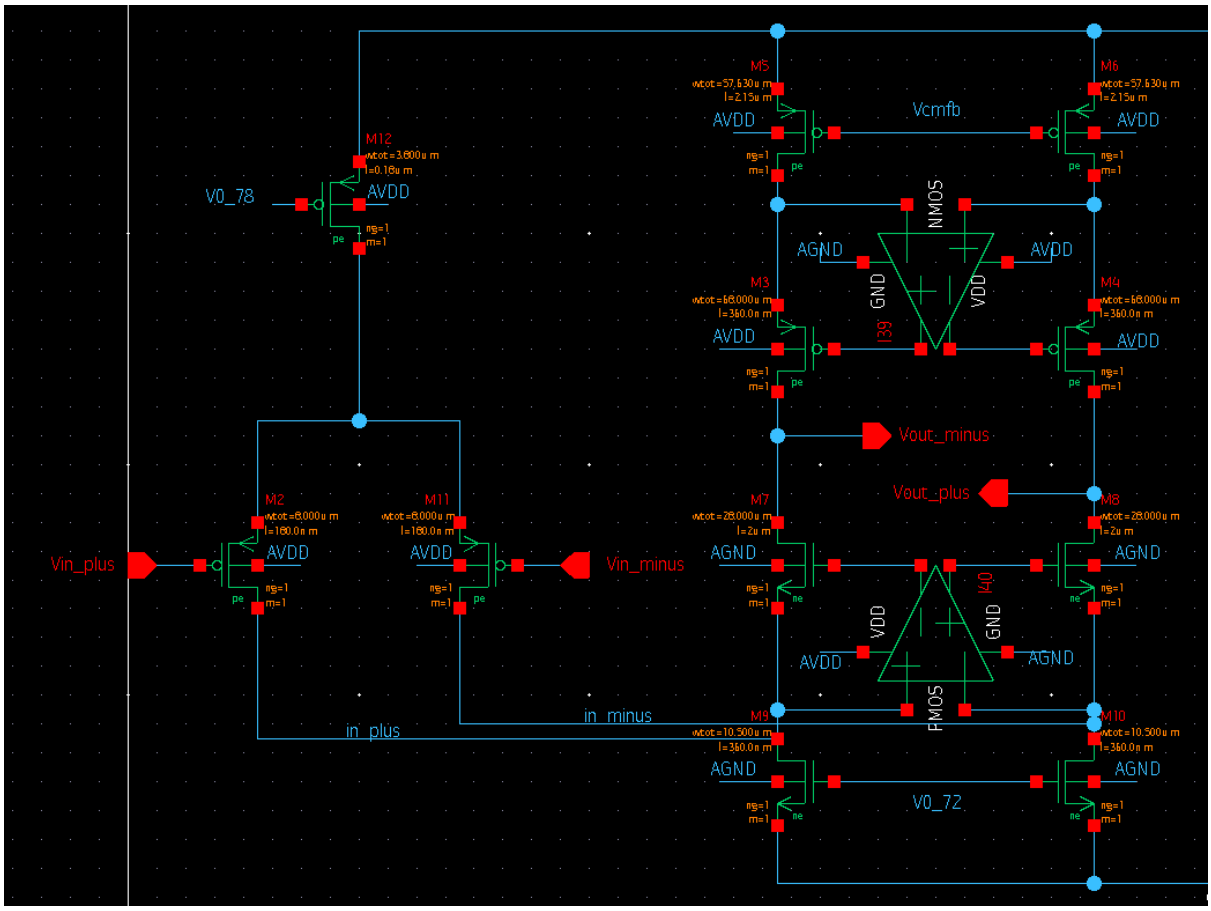

Figure 10: Fully differential folded cascode OTA schematic design with device parameters

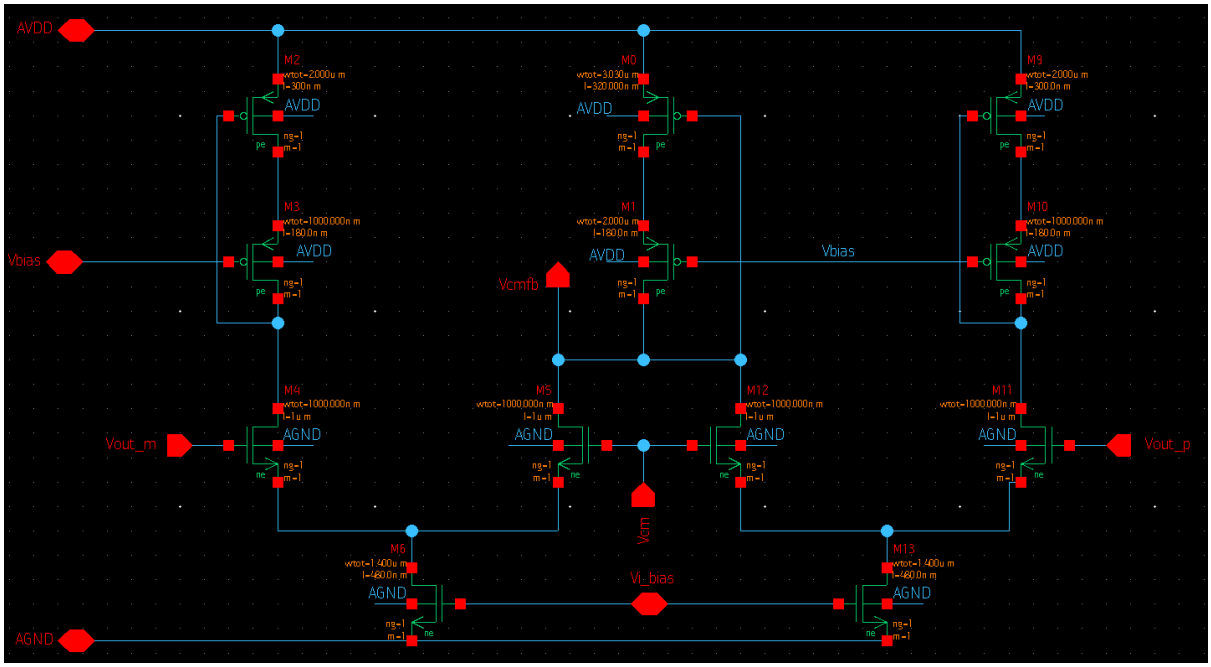

Figure 11: Common mode feedback circuit schematic design with device parameters

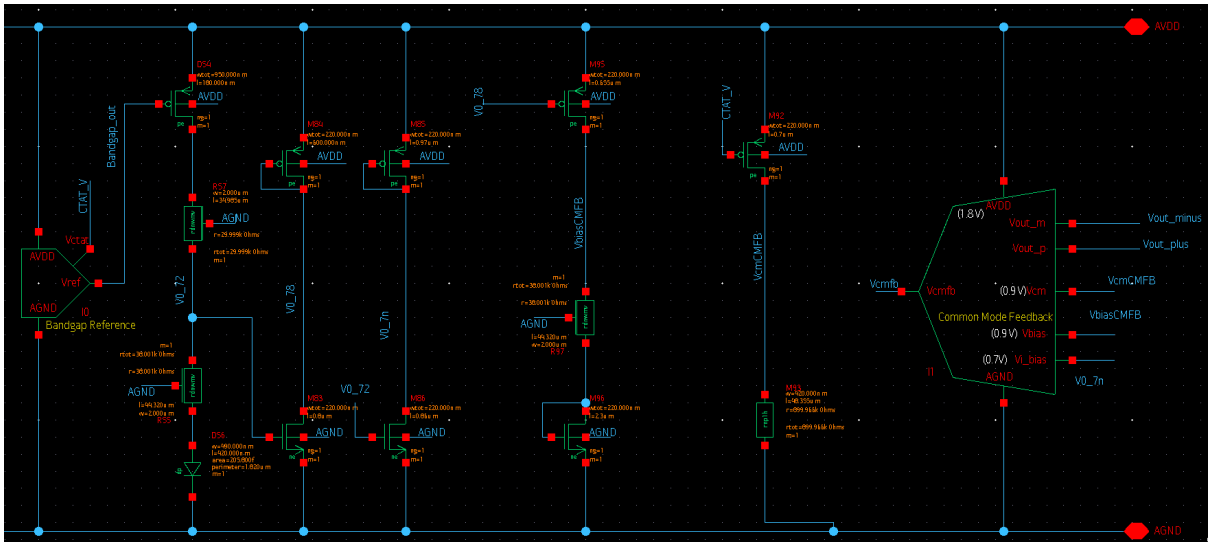

Figure 12: Bias network schematic design with device parameters

5.2 Fully Differential Folded Cascode OTA Operating Points

Similar to previous subsection, operating points are also presented in three subcircuits.

At 25 C° amplifier circuit (including gain boosting amplifiers) consumes 44.24153μA of current. Common mode feedback circuit consumes 8.21385μA and bias network (excluding bandgap reference circuit) consumes 4.043526 μA. Thus total current consumption of full differential folded cascode OTA is 56.498906 μA, which corresponds to 101.6980308 μW $\approx$ 101.7 μW of power consumption. Bandgap circuit consumes 7.38644 μA thus power consumption equals to 13.295592 μW $\approx$ 13.3 μW. And total current of symmetrical OTA is 33.83257 μA, corresponds to 60.898626 μW $\approx$ 60.9 μW. Total power consumption of the design is approximately equals to 175.9 μW at 25 C°.

5.2.1 Amplifier

Figure 13 provides node voltages and device currents for the amplifier subcircuit. DC voltage level at 25 C° for output nodes are 979.272 mV for V_{out_minus} and 979.264 mV for V_{out_plus}; showing a 8 μV offset. DC voltage levels for V_{out_plus} and V_{out_minus} are presented at figure 16. DC voltage level for output nodes vary between 865 mV to 985 mV with respect to temperature.

5.2.2 Common Mode Feedback Circuit

Operating points for common mode feedback circuit is presented at figure 14. Common mode feedback circuit generates a 1.0699 V of common mode feedback voltage, V_{cmfb}.

As argued before, all bias voltages (including V_{CM}) optimised to achieve highest temperature independence.

5.2.3 Bias Network

Figure 15 presents the operating points of the bias network of the fully differential folded cascode OTA. As discussed before, bias voltages designed to show specific behaviour with respect to temperature as well as voltage values.

Unfortunately net names at figure 15 does not represent their voltage level at 25 C°. That is because the voltage levels were also optimised, but the net names left unchanged. Moreover, a V_{ctat} output is added to the bandgap reference circuit. V_{ctat} provides counterproportional to absolute temperature

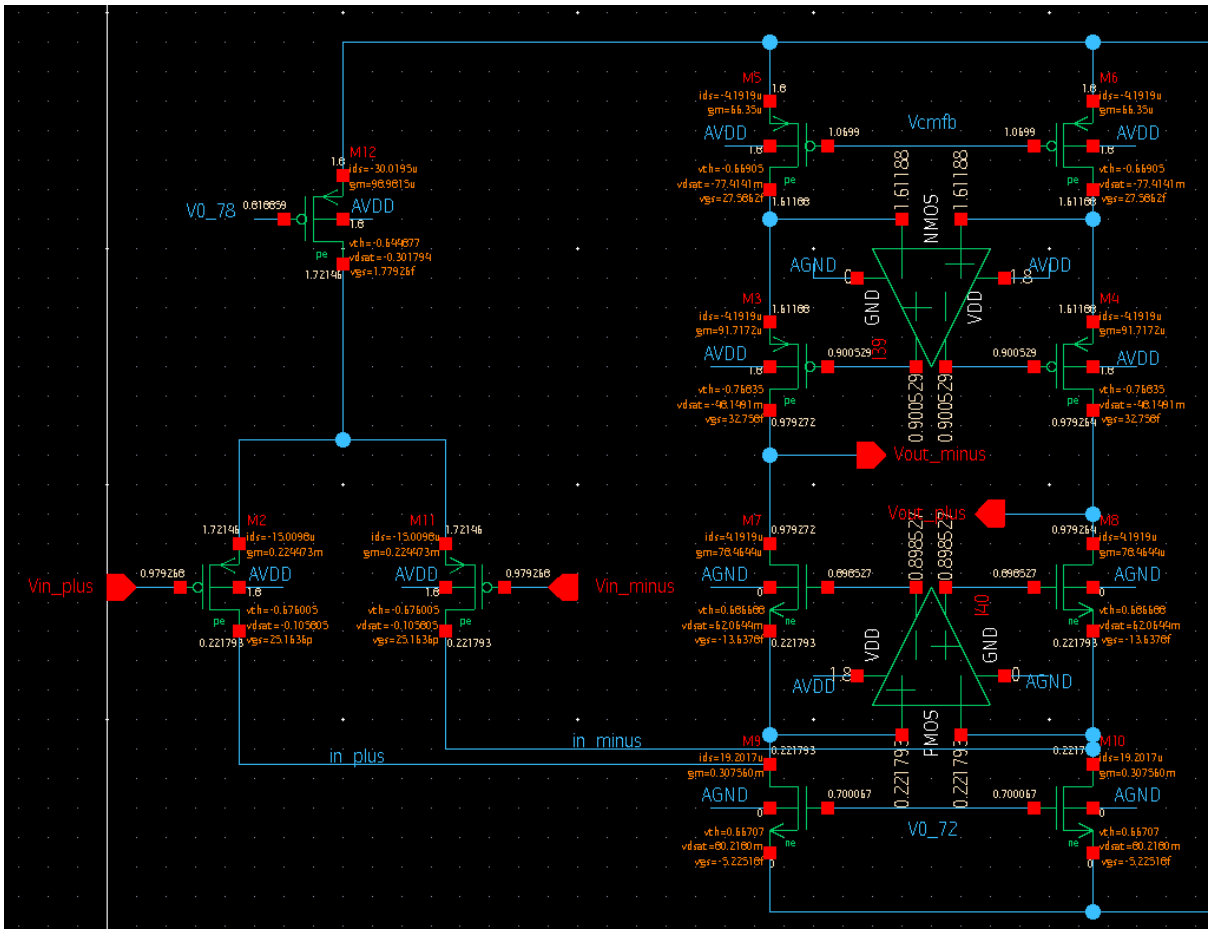

Figure 13: Fully differential folded cascode OTA schematic design with operating points

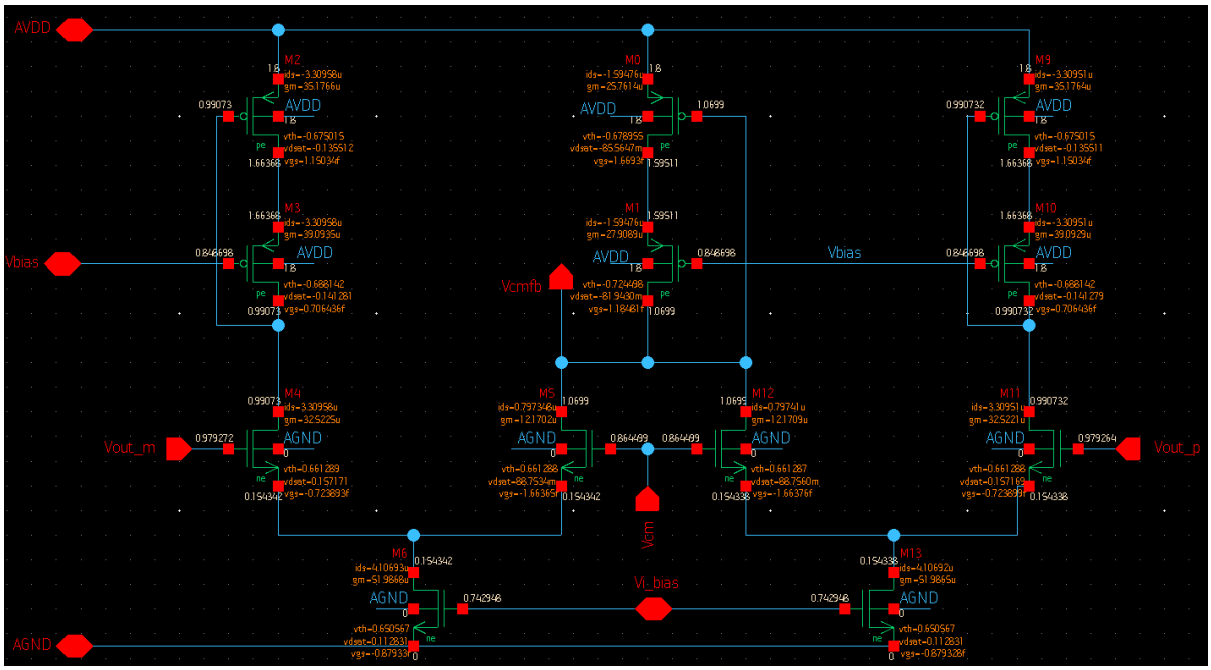

Figure 14: Common mode feedback circuit schematic design with operating points

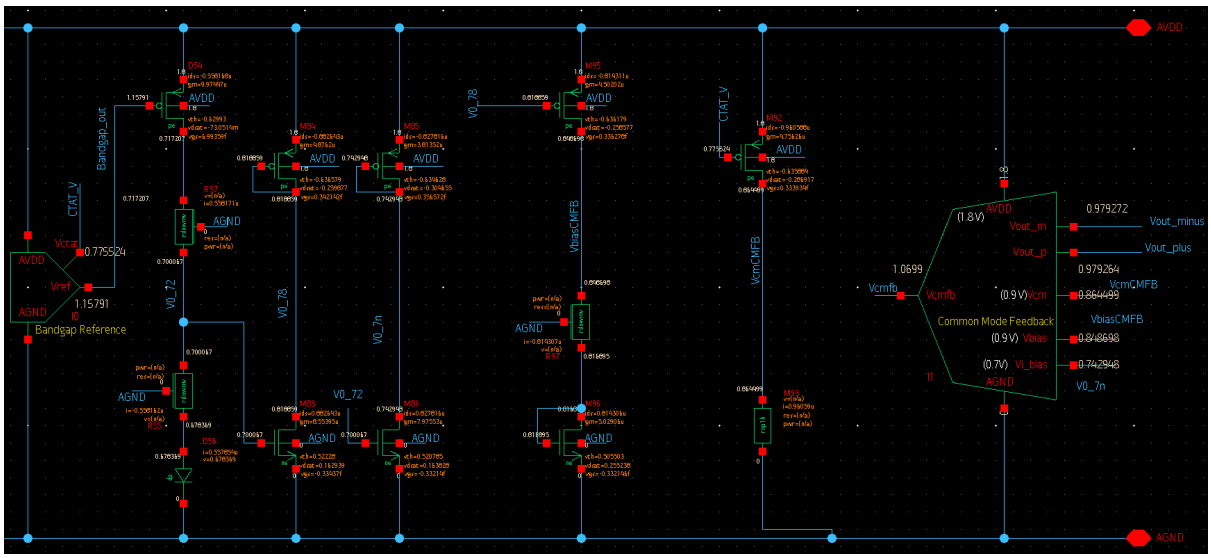

Figure 15: Bias network schematic design with operating points

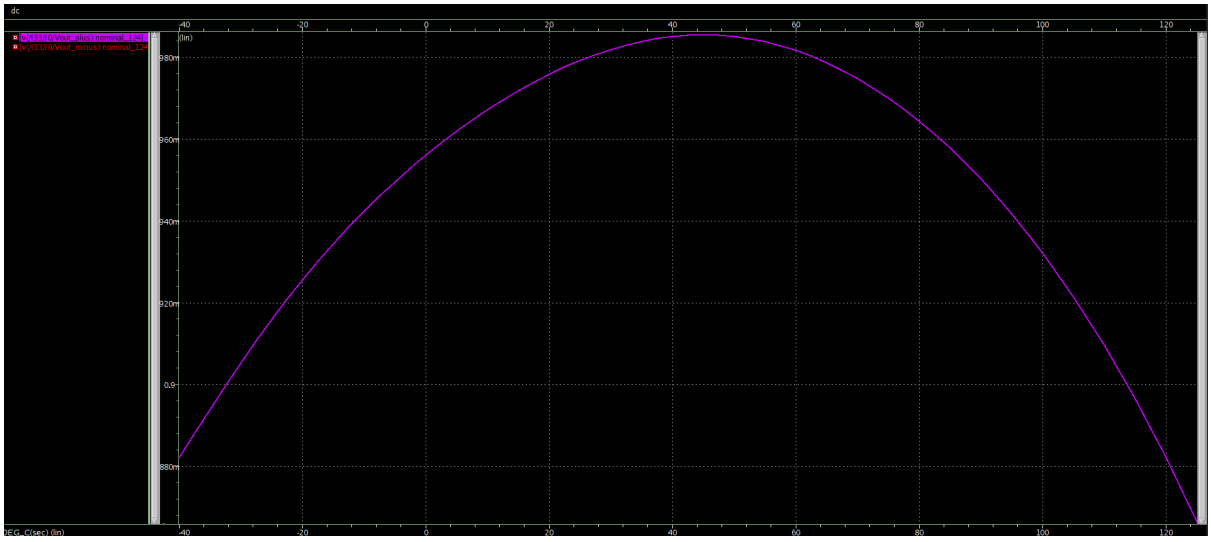

Figure 16: DC voltage level of V_{out} of fully differential folded cascode OTA

voltage reference as the name suggests. It is taken from the output of the OTA used at the bandgap reference circuit.

5.3 Fully Differential Folded Cascode OTA Simulation Results

Table 5: Fully Differential Folded Cascode OTA Simulation Results

Output	Value	Unit	Expression	Analysis
Open Loop Gain	103.641	dB	db20(ymax(v(/Vout_ac)))	AC
PSRR GND	-88.6963	dB	db20(ymin(v(/Vpsrr_gnd)))	AC
PSRR VDD	-80.0152	dB	db20(ymin(v(/Vpsrr_Vdd)))	AC
Phase Margin	75.9039	degree	phase_m(v(/Vout_ac),1)	AC
3dB Bandwidth	106.942	Hz	bw3db(v(/Vout_ac))	AC
Output Resistance	344.906M	Ω	(ymax(v(/Vout_res))	AC
Unity Gain Bandwidth	16.01M	Hz	bw(v(/Vout_ac), db20(ymax(v(/Vout_ac))))	AC

Table 5 provides typical simulation results for fully differential folded cascode OTA. Design provides 16.01 MHz unity gain bandwidth. Power rejection ratios are -88.7 dB and -80 dB for ground and VDD respectively. Figure 17 provides AC simulation result at 25 C°. Design provides 103.6 dB open loop gain and 75.9° phase margin.

Figure 18 provides open loop gain and phase margin with respect to temperature. Design provides a open loop gain around 103.2 dB with maximum ± 1.5 dB variation between -40 C° and 125 C°. Phase margin of the design is around 71° with maximum ± 5° variation between -40 C° and 125 C°.

Table 6: Fully Differential Folded Cascode OTA Corner Simulation Results

Output	Unit	Violations	Minimum	Maximum	Mean	Standard Deviation
Open Loop Gain	dB	29/45	-59.5480	105.263	60.4713	48.4516
PSRR GND	dB	-	-207.847	-11.8194	-108.789	57.6916
PSRR VDD	dB	-	-205.557	-4.40259	-115.227	55.9715
Phase Margin	degree	17/45	43.0693	138.558	85.2508	20.8099
3dB Bandwidth	Hz	-	10.4246	73.5102M	10.7147M	17.4711M
Output Resistance	Ω	-	1.26741k	3.53794G	465.403M	664.114M
Unity Gain Bandwidth	Hz	45/45	21.1256k	35.117M	12.3939M	10.7605M

Table 6 provides corner simulation results. For corner simulations following three goals were set:

- Open loop gain > 100 dB
- Phase margin > 70°
- Unity gain bandwidth > 200 MHz

Design provides good resistance against temperature changes. However, it is vulnerable to changes at the supply voltage. Thus, it fails on some of the corners. Unity gain bandwidth goal is never satisfied.

6 Gain Boosting OTAs

This section will present schematic design of gain boosting OTA. Moreover, DC operating points are presented in this section. However, AC or transient simulation results of gain boosting OTAs are not discussed in this report.

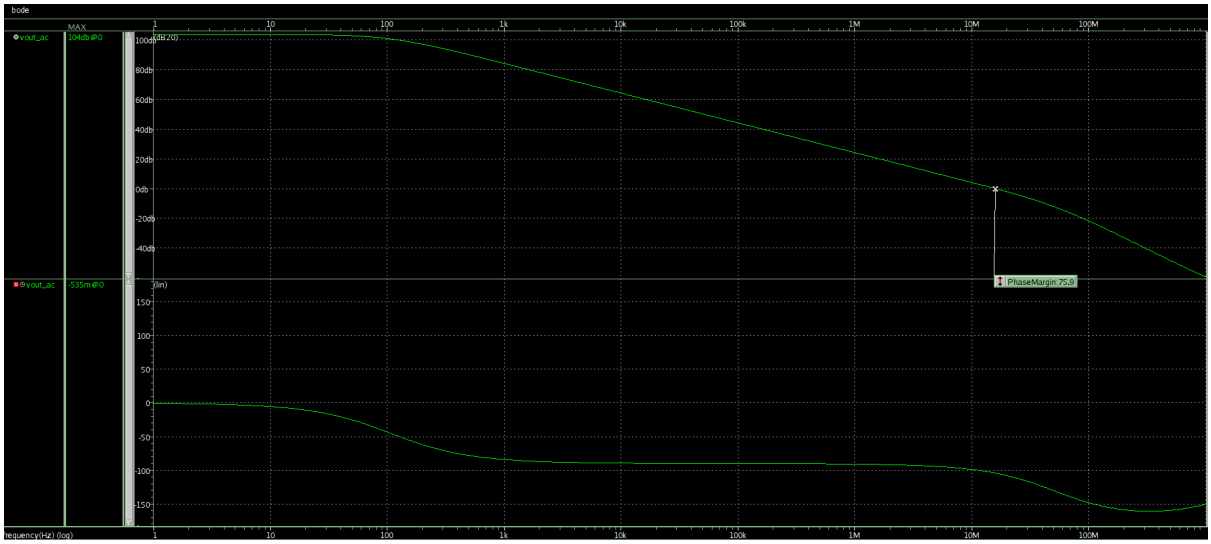

Figure 17: Typical AC simulation result for fully differential folded cascode OTA

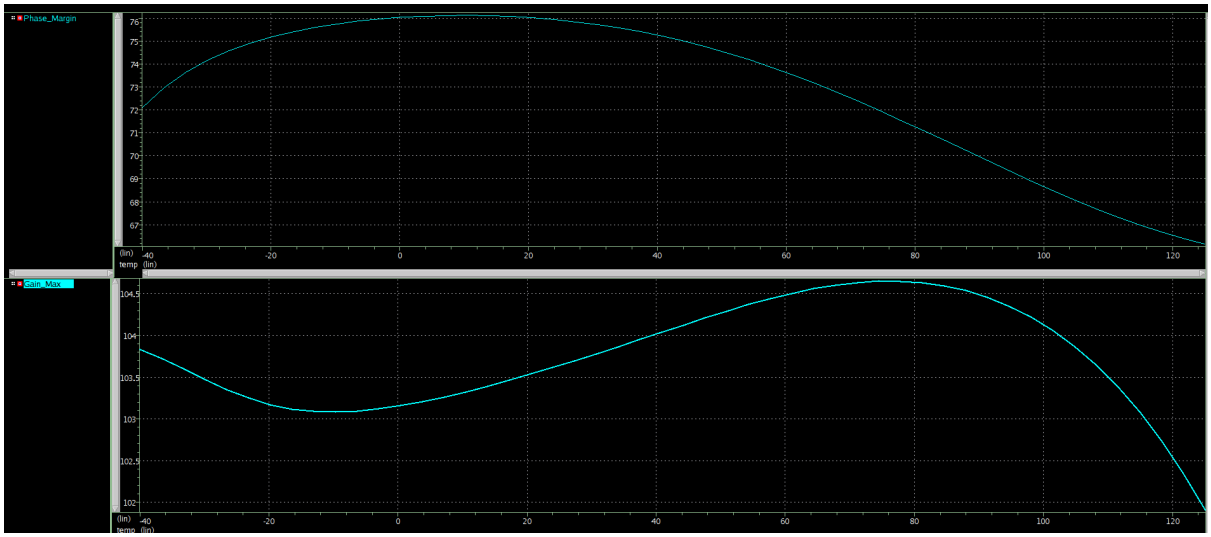

Figure 18: Maximum open loop gain and phase margin of fully differential folded cascode OTA with respect to temperature

6.1 NMOS Input Gain Boosting OTA

Figure 19 provides device parameters of NMOS input gain boosting OTA and figure 20 provides operating points.

6.2 PMOS Input Gain Boosting OTA

Figure 21 provides device parameters of PMOS input gain boosting OTA and figure 22 provides operating points.

7 Conclusion

This report presents the design of fully differential folded cascode OTA. Moreover, design of the components used in the fully differential folded cascode OTA is presented. These components are a bandgap reference circuit, symmetrical OTA and gain boosting OTAs.

Fully differential folded cascode OTA design to provide stable gain with respect to temperature between -40 C° and 125 C°.

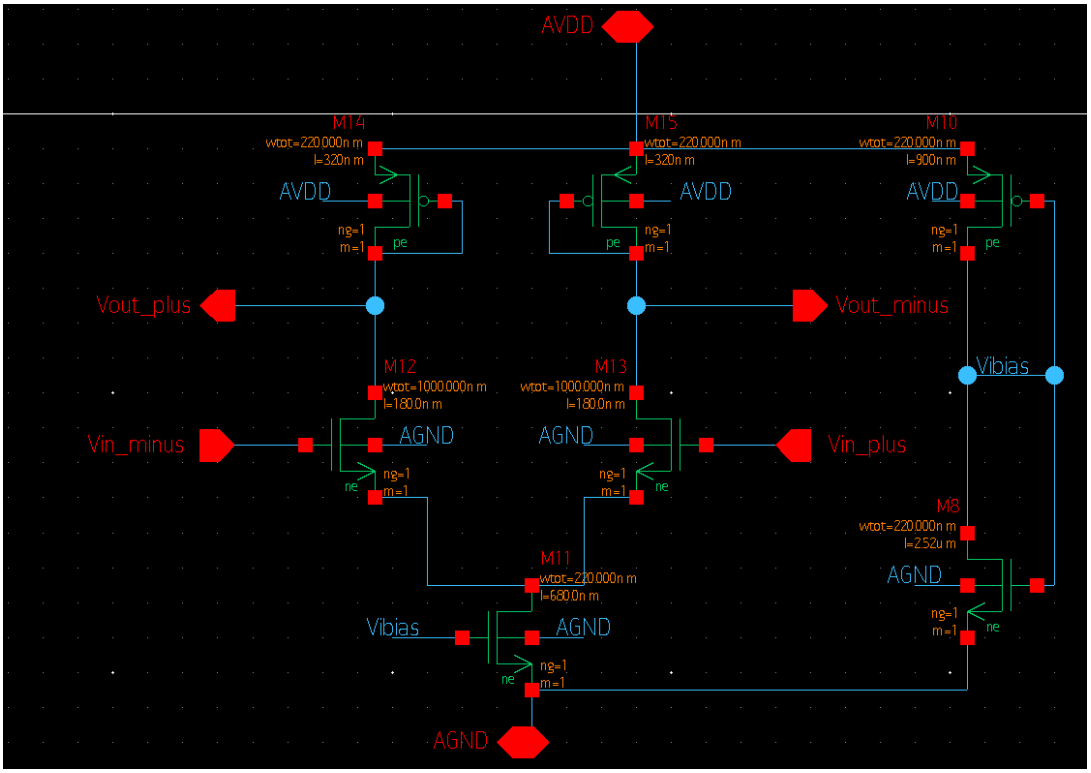

Figure 19: NMOS input gain boosting OTA device parameters

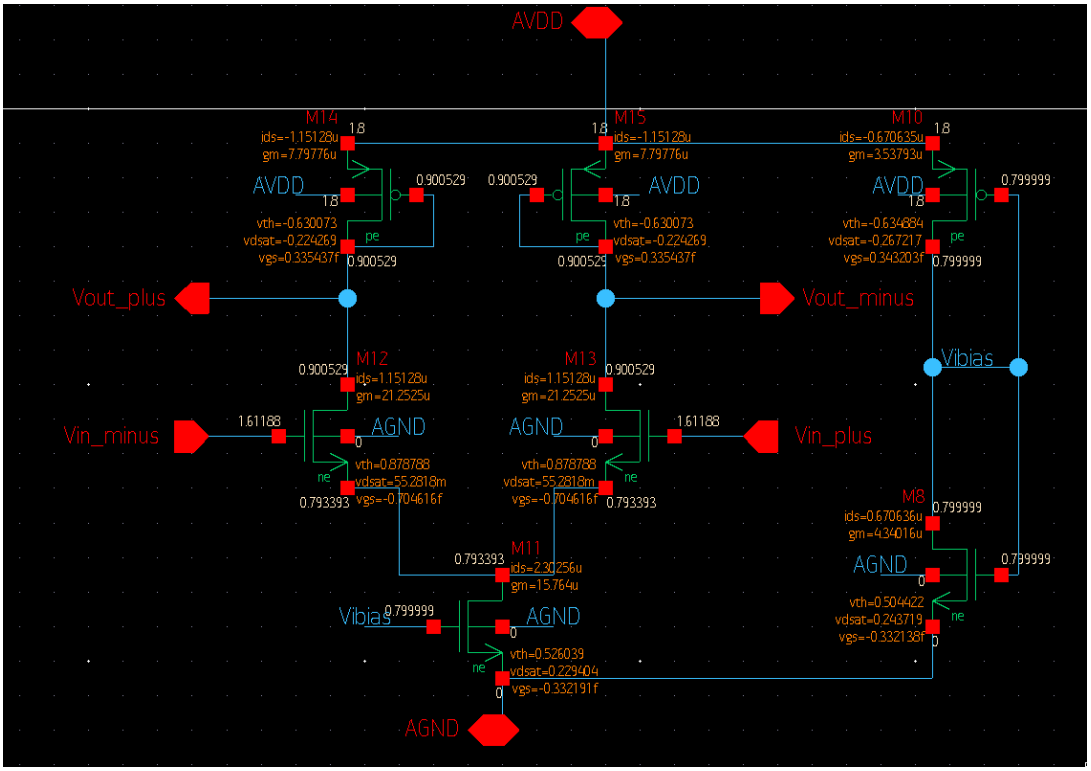

Figure 20: NMOS input gain boosting OTA operating points

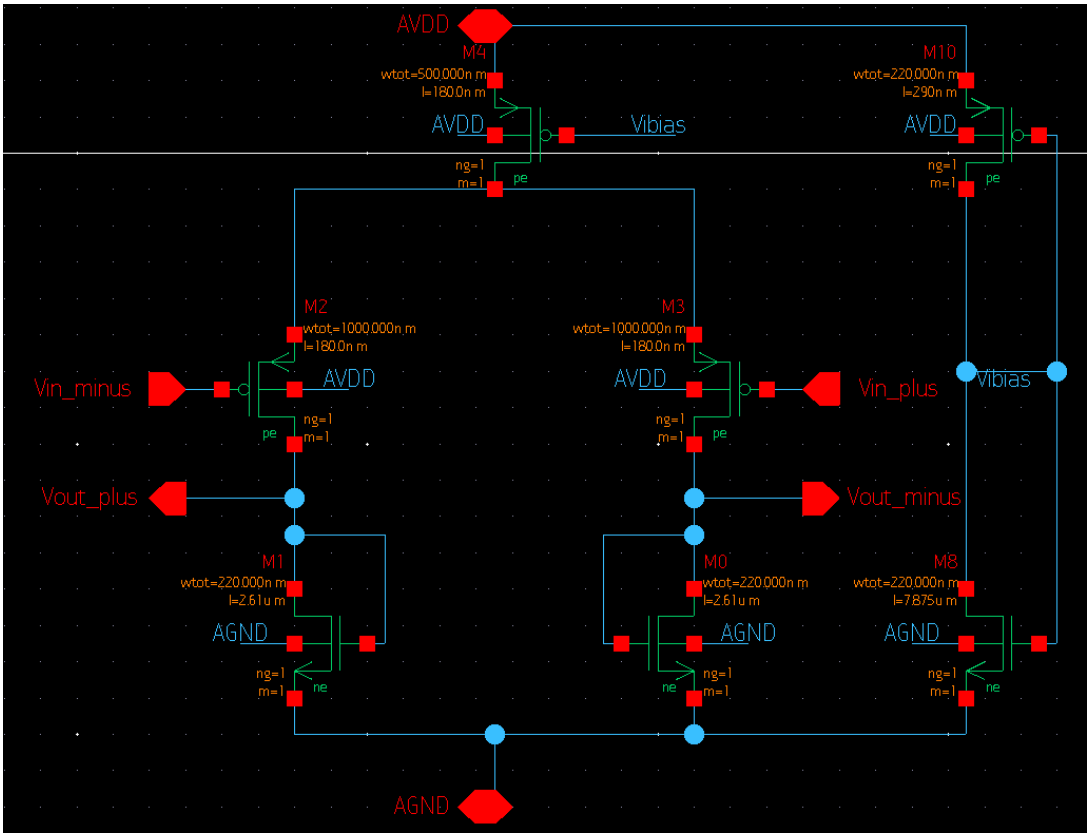

Figure 21: PMOS input gain boosting OTA device parameters

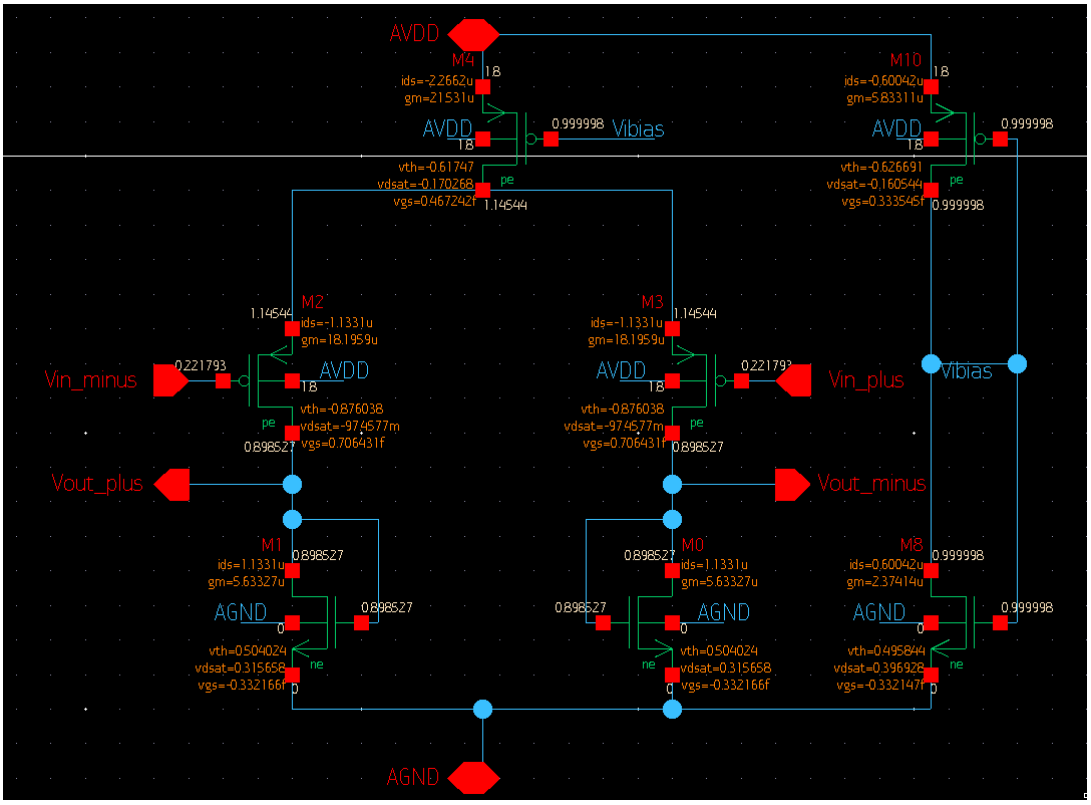

Figure 22: PMOS input gain boosting OTA operating points

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